FAST

Fairchild Advanced Schottky TTL

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Introduction

This is an introductory brochure for Fairchild Advanced Schottky TTL, FAST, a family of TTL circuits that exhibits a combination of performance and efficiency unapproached by any other TTL family. Made with the proven Isoplanar process, 54F/74F circuits offer the switching speed and output drive capability of Schottky TTL, with superior noise margins and only one-fourth the power consumption.

Section 1 Product Index/Availability Guide
Lists 54F/74F circuits currently planned, together with their scheduled introduction dates. More circuits will be added as market needs are identified.

Section 2 Family Characteristics
Discusses FAST circuit characteristics and noise margins and contains family ratings, dc specifications and ac waveforms.

Section 3 Circuit Selection Guides
Contains pinouts, features and functional descriptions; circuits are grouped functionally rather than numerically.

Section 4 Data Sheets
Contains full data sheets for SSI gates and flip-flops.

Section 5 Ordering Information and Package Outlines
The simplified purchasing code which identifies not only the device type, but also the package type and temperature range, is explained. Detailed physical dimension drawings for each package are given.

Section 6 Field Sales Offices, Representatives and Distributor Locations

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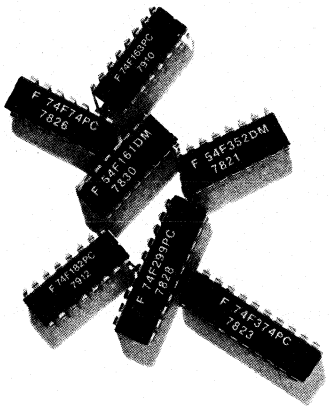

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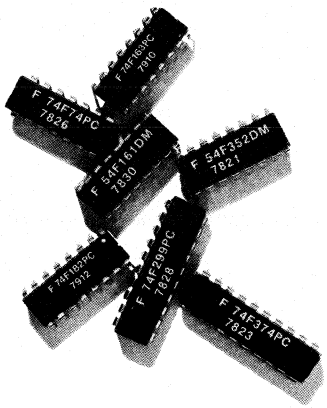


Section 2 Circuit Characteristics

FAST Technology
FAST is an acronym for Fairchild Advanced Schottky TTL. FAST circuits are made with the advanced Isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz. Isoplanar is an established Fairchild process, used for years in the manufacture of bipolar memories, CMOS, subnanosecond ECL and I^{3}L™ (Isoplanar Intergrated Injection Logic) LSI devices.

In the Isoplanar process, components are isolated by a selectively grown thick oxide rather than the P^+ isolation region used in the Planar process. Since this oxide needs no separation from the base-collector regions, component and chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

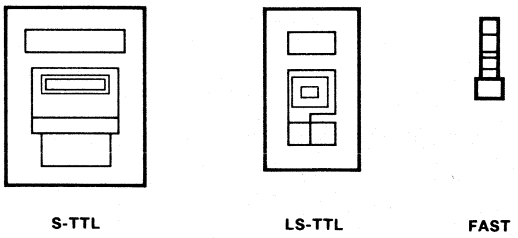


Fig. 2-1 Relative Transistor Size in Various TTL Families

Figure 2-1 shows the relative size of phase-splitter transistors (Q2 in *Figure 2-3*) used in Schottky, Low Power Schottky and FAST circuits. The LS-TTL transistor is smaller than that of S-TTL because of process refinements, shallower diffusions and smaller operating currents. The relative size of the FAST transistor illustrates the remarkable reduction afforded by the Isoplanar process. This in turn reduces junction capacitances, while the oxide isolation reduces side-wall capacitance. The effect of these reductions is an increase in frequency response by a factor of three or more. *Figure 2-2* shows the frequency response of two sizes of transistors made with the Isoplanar II process. Because they have modest, well-defined loads and thus can use smaller, faster transistors, internal gates of MSI devices are faster than SSI gates such as the 74F00 or 74F02. SSI gates, on the other hand, are designed to have high output drive capability and thus use larger transistors.

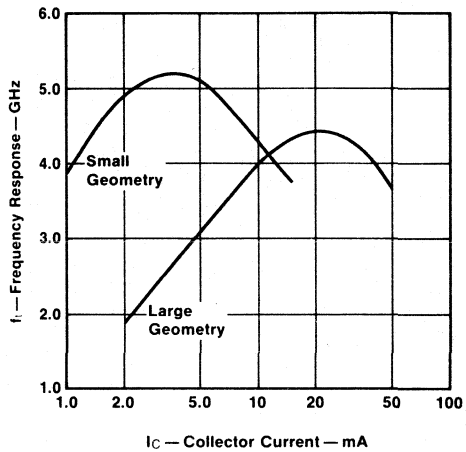


Fig. 2-2 Isoplanar Transistor Frequency Response

FAST Circuitry

The 2-input NAND gate, shown in *Figure 2-3*, has three stages of gain (Q1, Q2, Q3) instead of two stages as in other TTL families. This raises the input threshold voltage and increases the output drive. The higher threshold makes it possible to use pn diodes for the input AND function (D1 and D2) and still achieve an input threshold of 1.5 V. The capacitance of these diodes is comparatively low, which results in improved ac noise immunity. The effect of the threshold adjustment can be seen in the voltage transfer characteristics of *Figures 2-4, 2-5* and *2-6*. At 25°C (*Figure 2-5*) the FAST circuit threshold is nearly centered between the 0.8 V and 2.0 V limits specified for TTL circuits. This gives a better balance between the HIGH- and LOW-state noise margins. The +125°C characteristics (*Figure 2-6*) show that the FAST circuit threshold is comfortably above the 0.8 V specification, more so than in S-TTL or LS-TTL circuits. At -55°C, the FAST circuit threshold is still well below the 2.0 V specification, as shown in *Figure 2-4*.

The effect of the FAST circuit threshold placement is shown in the pulse noise immunity curves of *Figure 2-7*. These characteristics were determined by measuring the various combinations of input pulse amplitude and duration required to cause the gate output to fall to the 2.0 V level. The higher threshold of FAST circuits gives them a clear advantage in noise immunity over S-TTL and LS-TTL circuits.

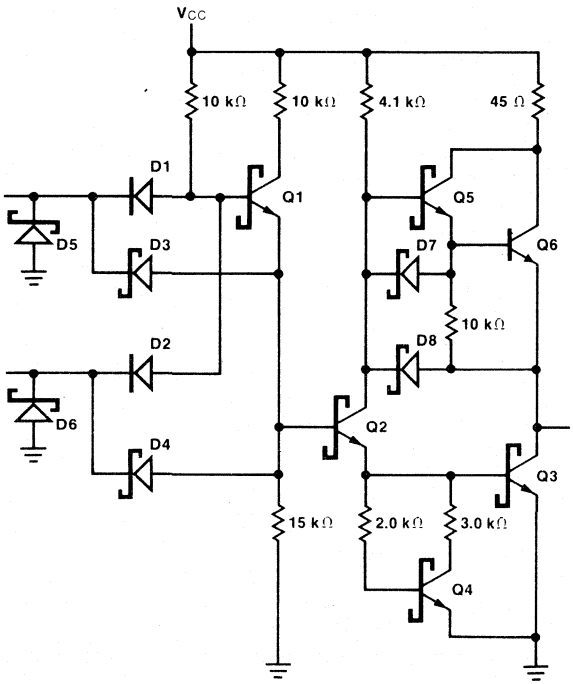


Fig. 2-3 Basic FAST Gate Schematic

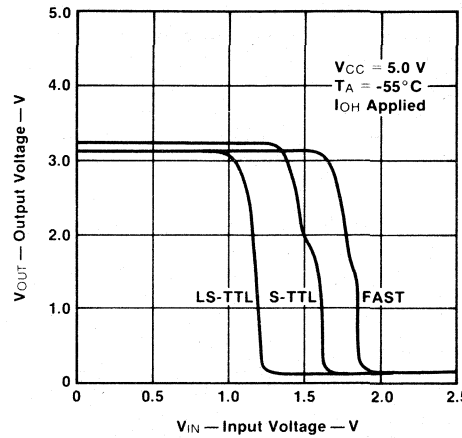


Fig. 2-4 Transfer Functions at Low Temperature

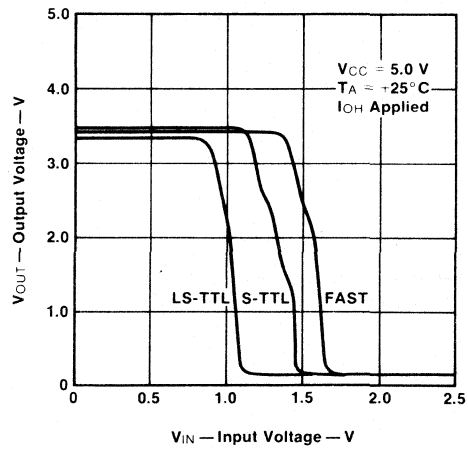


Fig. 2-5 Transfer Functions at Room Temperature

FAST circuits contain several speed-up diodes to help discharge internal capacitances. Referring again to *Figure 2-3*, when a HIGH-to-LOW transition occurs at the D1 input, for example, Schottky diode D3 acts as a low-resistance path to discharge the several parasitic capacitances connected to the base of Q2. This effect only comes into play, however, as the input signal falls below about 1.2 V; D3 does not act as an entry path for negative spikes superimposed on a HIGH input level. When Q2 turns on and its collector voltage falls, D7 provides a discharge path for capacitance at the base of Q6. Whereas D3, D4 and D7 enhance switching speed by helping to discharge internal nodes, D8 contributes to the ability of a FAST circuit to rapidly discharge load capacitance. Part of the charge stored in load capacitance passes through D8 and Q2 to increase the base current of Q3 and increase Q3's current sinking capability during the HIGH-to-LOW output voltage transition.

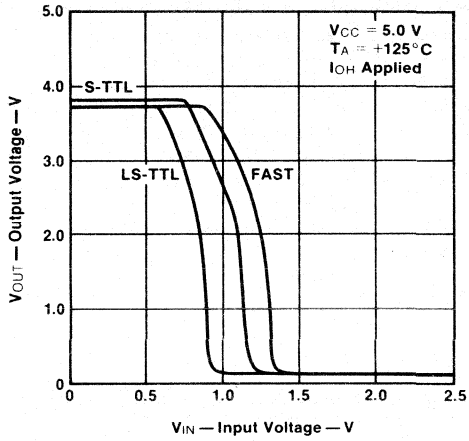


Fig. 2-6 Transfer Functions at High Temperature

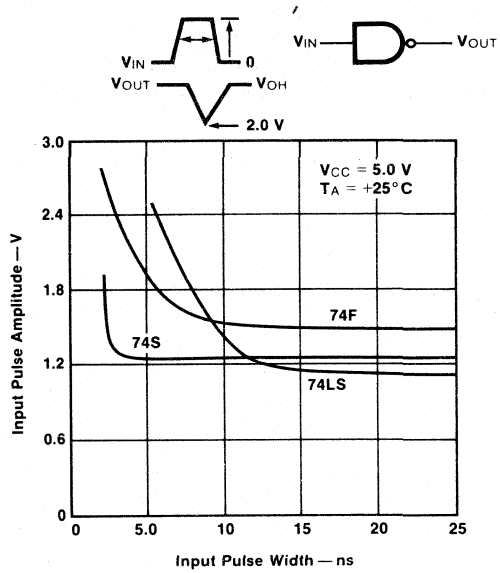


Fig. 2-7 Pulse Noise Immunity Comparison

The Schottky clamping diodes built into the transistors prevent saturation, thereby eliminating storage time as a factor in switching speed. Similarily, the speed-up diodes tend to minimize the impact of other variables on switching speed. The overall effect is to minimize variation in switching speed of FAST circuits with variations in supply voltage and ambient temperature (*Figures 2-8* through *2-11*). Propagation delay is specified not only under nominal supply voltage and temperature conditions, but also over the recommended operating range of V_{CC} and T_A for both military and commercial grade devices.

The internal switching speed of a logic circuit is only one aspect of the circuit's suitability for high-speed operation at the system or subsystem level; the other aspect is the ability of the circuit to drive load capacitance. FAST circuit outputs are structured to sink at least 20 mA in the LOW state, the same as S-TTL. This capability plus the effect of the aforementioned feedback through D8 assures that the circuit can rapidly discharge capacitance. During a LOW-to-HIGH transition, the pull-up current is limited by the 45 Ω resistor, versus 55 Ω for S-TTL.

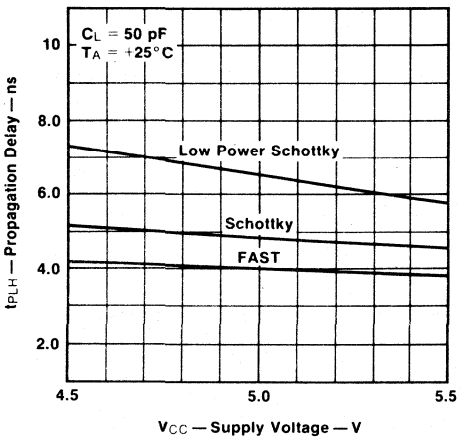


Fig. 2-8 Propagation Delay t_{PLH} vs V_{CC}

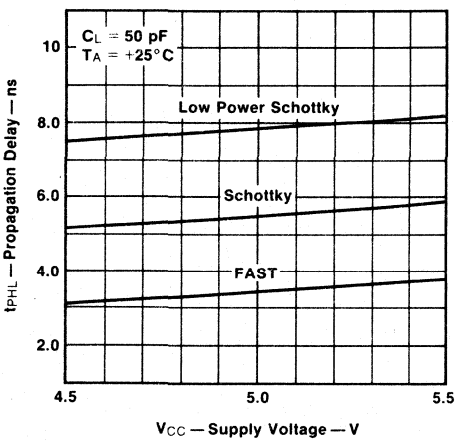


Fig. 2-9 Propagation Delay t_{PHL} vs V_{CC}

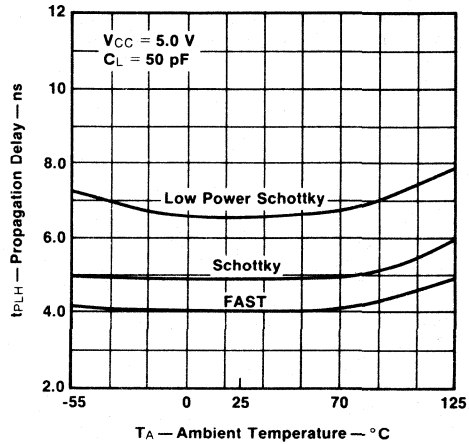


Fig. 2-10 Propagation Delay t_{PLH} vs Temperature

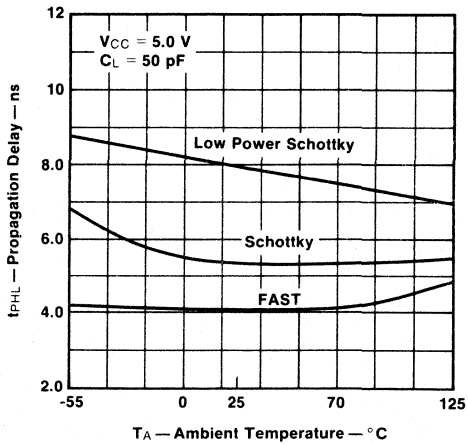


Fig. 2-11 Propagation Delay t_{PHL} vs Temperature

Therefore, FAST circuits are inherently more capable than S-TTL of charging load capacitance. *Figures 2-12* and *2-13* indicate the effect of load capacitance on propagation delays and transition times of FAST circuits. *Figure 2-14* shows the typical output LOW voltage V_{OL} as a function of load current. The typical I-V characteristic in the quiescent HIGH state is shown in *Figure 2-15*. In the lower left, the intercept along the vertical axis indicates the short-circuit output current I_{OS}. From this point to approximately -10 mA, the slope is about 50 Ω, indicating that the totem-pole pull-up is saturated and current is limited principally by the 45 Ω resistor. From -10 mA upward almost to the horizontal axis, the slope is the dynamic output resistance of transistor Q6. That part of the characteristic in the upper right shows that a bi-state output cannot be pulled up much above V_{CC} because of the sneak path through D8 and the 4.1 kΩ resistor back to V_{CC}.

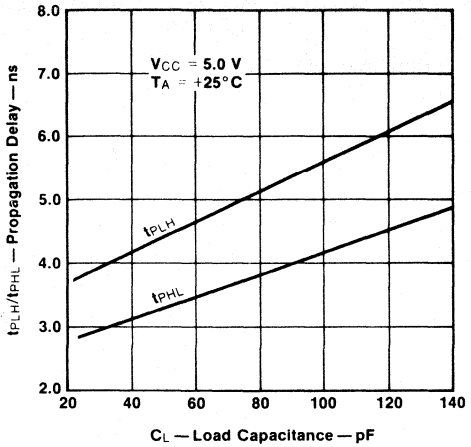


Fig. 2-12 Propagation Delay vs Load Capacitance

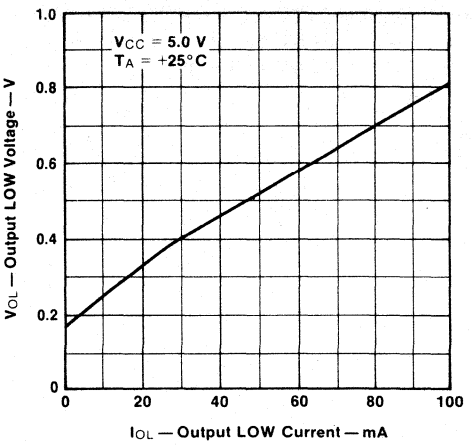


Fig. 2-14 Output LOW Characteristic

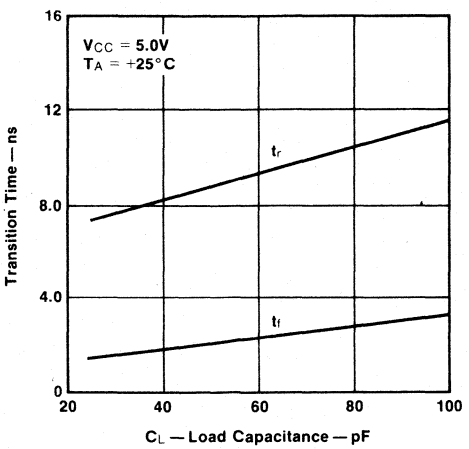


Fig. 2-13 Transition Time vs Load Capacitance

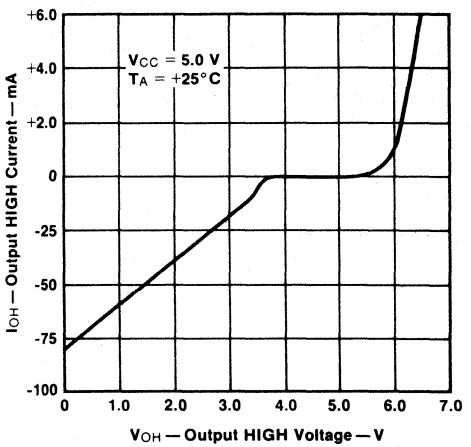


Fig. 2-15 Output HIGH Characteristic

A typical input I-V characteristic is shown in *Figure 2-16*. An input clamping diode (D5 or D6 in *Figure 2-3*) conducts if an input signal tends to go more negative than about -0.4 V. This limits the undershoot that might occur at the end of a long line following a HIGH-to-LOW transition. The clamping diodes in FAST circuits have been improved over those used in LS-TTL to prevent parasitic coupling through sneak paths to other components on the chip. For input voltage in the range of -0.4 V to about +1.5 V, the input current is governed principally by the 10 kΩ pull-up resistor of the input gate. With V_{CC} at the recommended maximum (+5.5 V or +5.25 V) and the input at +0.4 V, the specified maximum input current is 0.6 mA. This compares favorably with the 0.4 mA specified maximum for LS-TTL and is far below the 2.0 mA maximum for an S-TTL input. Thus, in a system comprised of FAST devices, there is less need for buffering to increase fan-out.

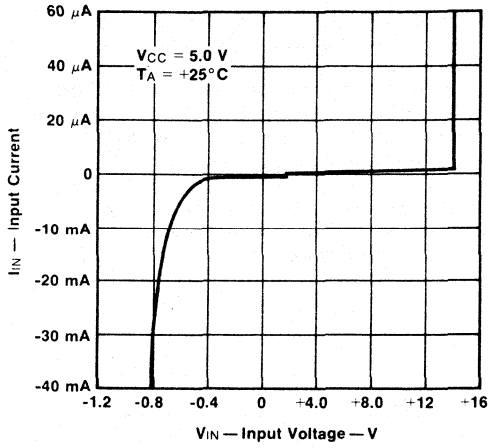


Fig. 2-16 Input Characteristic

Unit Loads (U.L.)

For convenience in system design, the input loading and fan-out characteristics of each circuit are specified in terms of unit loads. One unit load in the HIGH state is defined as 40 μA; thus both the input HIGH leakage current I_{IH} and the output HIGH current-sourcing capability I_{OH} are normalized to 40 μA. The specified maximum I_{IH} for a standard FAST input is 20 uA, or 0.5 U.L., while the I_{OH} rating for a standard output is 1.0 mA, or 25 U.L. Similarly, one unit load in the LOW state is defined as 1.6 mA and both the input LOW current I_{IL} and the output LOW current-sinking capability I_{OL} are normalized to 1.6 mA. The specified maximum I_{IL} for a standard FAST input is 0.6 mA, or 0.375 U.L., while the I_{OL} rating for a standard output is 20 mA, or 12.5 U.L. On the data sheets, the input and output load factors are listed in the Input Loading/Fan-Out Table. The table from the 54F/74F04 Hex Inverter is reproduced below.

In the right-hand column the input HIGH/LOW load factors are 0.5/0.375, with the first number representing I_{IH} and the second representing I_{IL}. For testing or procurement purposes, these load factors can easily be translated to actual test limits by multiplying them by 40 μA and 1.6 mA, respectively. The second set of numbers represents the rated output HIGH/LOW load currents I_{OH} and I_{OL}, respectively. The indicated HIGH/LOW drive factors of 25/12.5 translate to 1.0 mA and 20 mA by multiplying them by 40 μA and 1.6 mA, respectively.

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

Absolute Maximum Ratings[1]
(beyond which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage[2]	-0.5 V to +7.0 V
Input Current[2]	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State:	
Standard Output	-0.5 V to V_{CC} Value
3-State Output (with V_{CC} = 0 V)	-0.5 V to +5.5 V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL}

Recommended Operating Conditions[1]

	Min	Max
Free Air Ambient Temperature		
Military (XM)	-55°C	+125°C
Commercial (XC)	0°C	+70°C
Supply Voltage		
Military (XM)	+4.5 V	+5.5 V
Commercial (XC)	+4.75 V	+5.25 V

1. Unless otherwise restricted or extended by detail specifications.
2. Either input voltage or current limit sufficient to protect inputs.

54F/74F FAMILY DC CHARACTERISTICS[1]

SYMBOL	PARAMETER		LIMITS[2] Min	Typ[3]	Max	UNITS	V_{CC}[4]	CONDITIONS[2]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	Std.[6] Mil.	2.5	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std.[6] Com.	2.7	3.4				
		3-State	2.4	3.2				
V_{OL}	Output LOW Voltage			0.35	0.5	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input High Current, Breakdown Test, All Inputs				100	μA	Max	V_{IN} = 7.0 V
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.5 V
		0.75 U.L.			-1.2			
		n U.L.			n(-1.6)			
I_{OZH}	3-State Output OFF Current HIGH				20	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-20	μA	Max	V_{OUT} = 0.5 V
I_{OS}[5]	Output Short-Circuit Current	Standard[6]/ 3-State	-60		-150	mA	Max	V_{OUT} = 0 V
		Buffers/ Line Dvrs	-100		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.

AC Loading and Waveforms

Figure 2-17 shows the load circuit configuration used for ac testing of bi-state outputs. The appropriate value of C_L is shown on each individual data sheet in the ac table column headings. A pulse generator signal swing of 0 V to +3.0 V, terminated at the test socket, is recommended for ac testing. A 1.0 MHz square wave is recommended for most propagation delay tests, with rise and fall times of 2.5 ns. The generator pulse repetition rate must necessarily be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time, recovery time, etc. Low inductance type load capacitors are recommended for best correlation with factory test results.

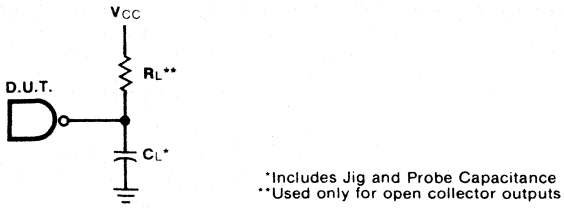


Fig. 2-17 Test Load for Bi-State Mode

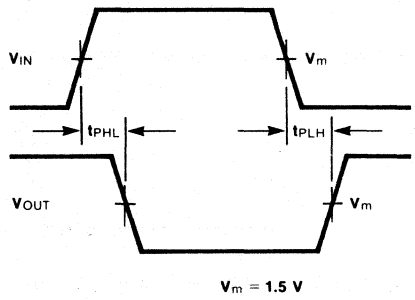


Fig. 2-18 Waveform for Inverting Functions

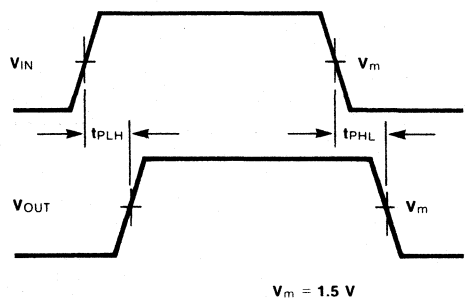


Fig. 2-19 Waveform for Non-Inverting Functions

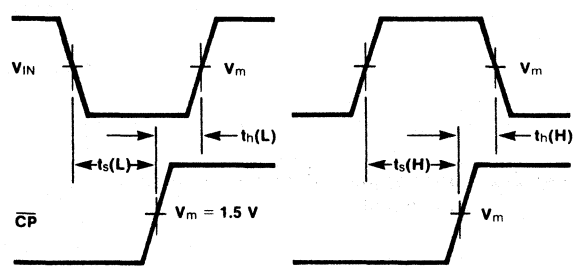


Fig. 2-20 Set-up and Hold Times, Rising-Edge Clock

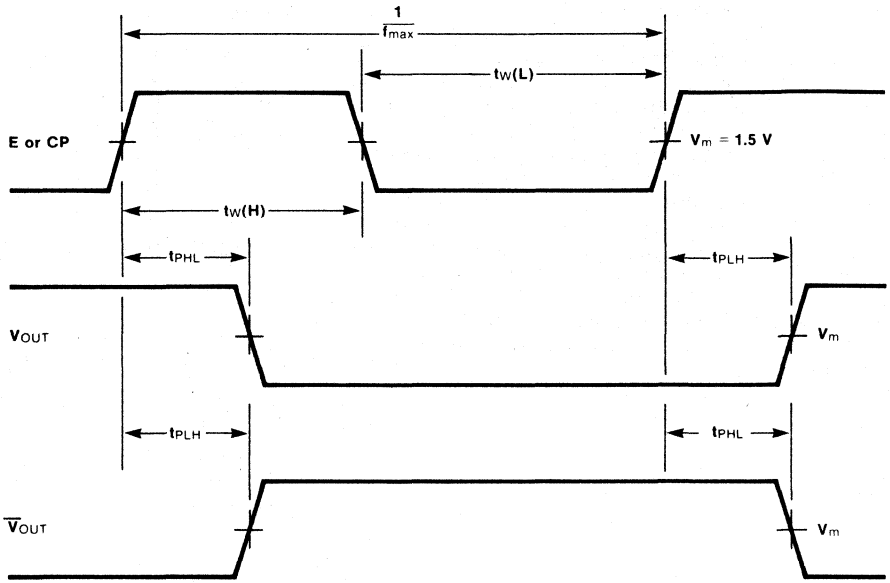


Fig. 2-21 Propagation Delays from Rising-Edge Clock or Enable

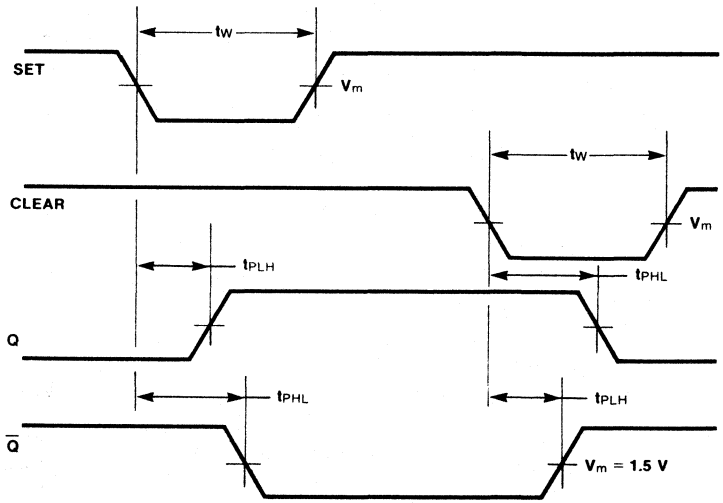
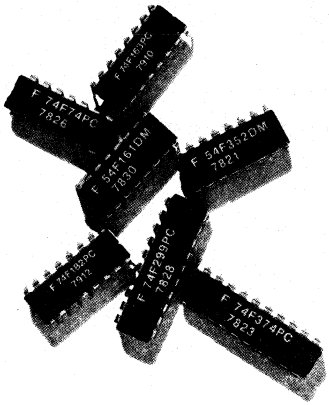
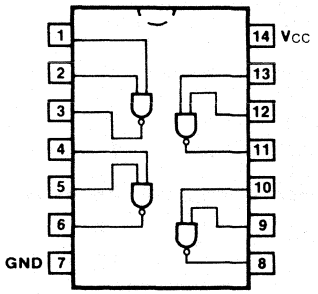


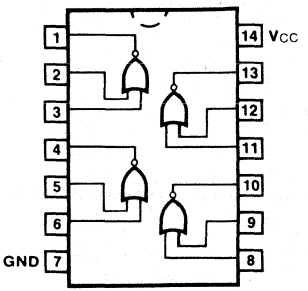
Fig. 2-22 Propagation Delays from Set and Clear (or Reset)



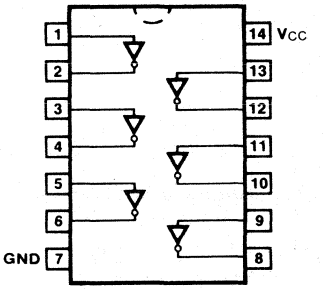
54F/74F00
Quad 2-Input NAND Gate



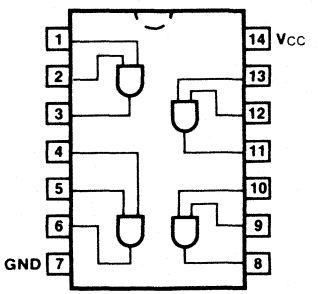
54F/74F02
Quad 2-Input NOR Gate



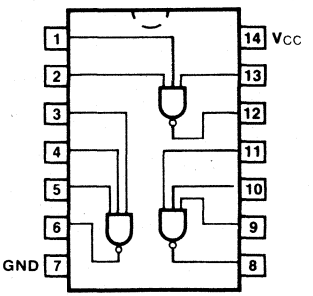
54F/74F04
Hex Inverter



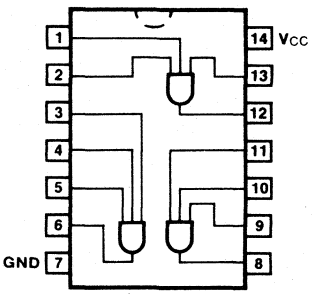
54F/74F08
Quad 2-Input AND Gate



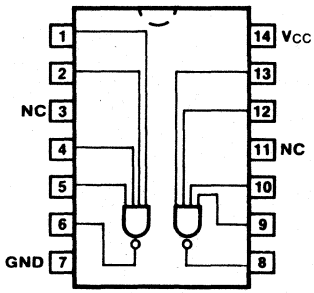
54F/74F10
Triple 3-Input NAND Gate



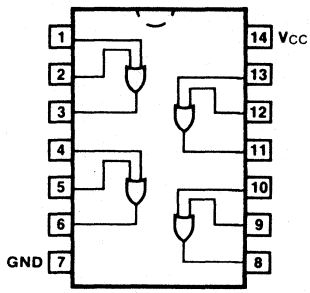
54F/74F11
Triple 3-Input AND Gate



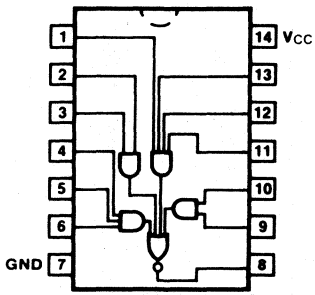
54F/74F20
Dual 4-Input NAND Gate



54F/74F32
Quad 2-Input OR Gate



54F/74F64
AND OR-Invert Gate



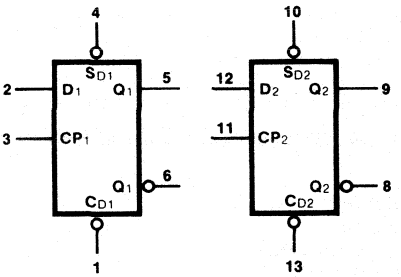
Dual D-Type Positive Edge-Triggered Flip-Flop

54F/74F74

Description — The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D input can change when the clock is in either state without affecting the flip-flop, provided that the D signal is in the desired state during the recommended setup and hold times relative to the rising edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{C}_D$ and $\overline{S}_D$ force both Q and $\overline{Q}$ HIGH.

Buffered Outputs
Fully Edge-Triggered
Overriding Direct Set and Clear
Clock Frequency 145 MHz Typ
Propagation Delay 4.8 ns Typ
Supply Current 10.5 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

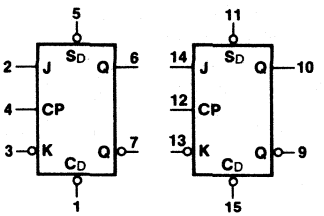
Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

54F/74F109

Description — The 'F109 contains two independent, high speed J$\overline{K}$ flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the rising edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and $\overline{K}$ inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the rising edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH. A D input is available by tying J and $\overline{K}$ together.

Buffered Outputs
Fully Edge-Triggered
Overriding Direct Set and Clear
Clock Frequency 140 MHz Typ
Propagation Delay 4.8 ns Typ
Supply Current 11.7 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

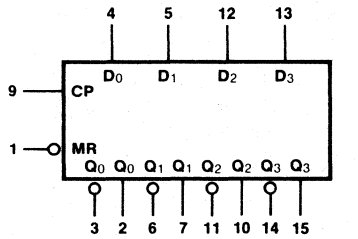
Quad D Flip-Flop

54F/74F175

Description — The 'F175 contains four high speed, edge-triggered D flip-flops with common Clock and Master Reset inputs, and individual D inputs and Q and $\overline{Q}$ outputs. Information on the D inputs is entered by the rising edge of the clock, provided that the recommended setup and hold times are observed. A LOW signal on $\overline{MR}$ forces all Q outputs LOW and $\overline{Q}$ outputs HIGH, independent of Clock or Data inputs.

True and Complement Outputs
Fully Edge-Triggered
Asynchronous Common Reset
Clock Frequency 150 MHz Typ
Propagation Delay 6.3 ns Typ
Supply Current 21 mA Typ

Logic Symbol



VCC = Pin 16
GND = Pin 8

Octal D-Type Flip-Flop

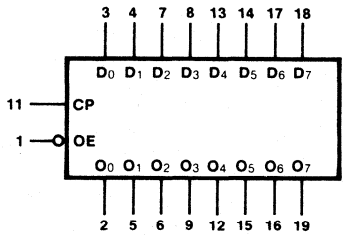
(With 3-State Outputs)

54F/74F374

Description — The 'F374 contains eight edge-triggered flip-flops with buffered 3-state outputs for bus oriented applications. Information on the D inputs is entered on the rising edge of the common Clock input, provided that the recommended setup and hold times are observed. A HIGH signal on the common Output Enable forces the outputs to the high impedance state but does not affect the state of the flip-flops or subsequent data entry.

Buffered 3-State Outputs
D-Type Inputs
Fully Edge-Triggered
Clock Frequency 110 MHz Typ
Propagation Delay 9.5 ns Typ
Supply Current 52 mA Typ

Logic Symbol



VCC = Pin 20
GND = Pin 10

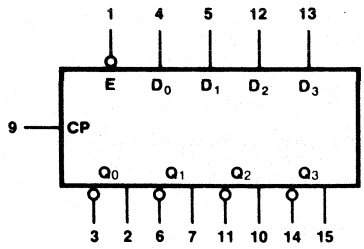
Quad Parallel Register 54F/74F379

(With Enable)

Description — The 'F379 storage register contains four edge-triggered flip-flops with individual D inputs and Q and $\overline{Q}$ outputs and with common Clock and input Enable inputs. Information present on the D inputs is entered on the rising edge of the clock, provided that $\overline{E}$ is LOW and the recommended setup and hold times are observed. When the $\overline{E}$ input is HIGH, the register retains the present data independent of the clock and D inputs.

Buffered Input Enable
Buffered Common Clock
Fully Edge-Triggered
Clock Frequency 150 MHz Typ
Propagation Delay 6.3 ns Typ
Supply Current 27 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

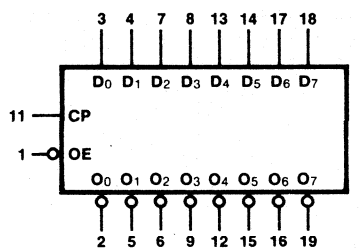
Octal D-Type Flip-Flop 54F/74F534

(With 3-State Outputs)

Description — The 'F534 contains eight edge-triggered flip-flops with individual D inputs and $\overline{Q}$ outputs, and with common Clock and 3-state Output Enable inputs. Information on the D inputs is entered on the rising edge of the clock, provided that the recommended setup and hold times are observed. A HIGH signal on $\overline{OE}$ forces the outputs to the high impedance state but does not affect the state of the flip-flops or subsequent data entry. The 'F534 is the same as the 'F374 but with inverted outputs.

Inverted 3-State Outputs
D-Type Inputs
Fully Edge-Triggered
Clock Frequency 110 MHz Typ
Propagation Delay 9.5 ns Typ
Supply Current 52 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

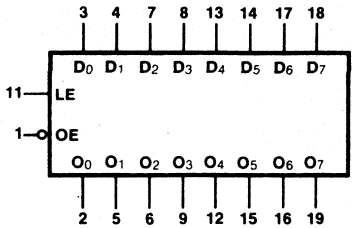
Octal Transparent Latch 54F/74F373

(With 3-State Outputs)

Description — The 'F373 contains eight D-type latches with 3-state outputs for bus organized applications. When the common Latch Enable input is HIGH the latches are transparent, i.e. an output will change state each time its D input changes. When LE is LOW, the data that meets the recommended setup and hold times is latched. A HIGH signal on the common Output Enable input forces the outputs to the high impedance state but does not affect the state of the latches or subsequent data entry.

Buffered 3-State Outputs
D-Type Inputs
Transparent Latches
Propagation Delay 6.0 ns Typ
Supply Current 46 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

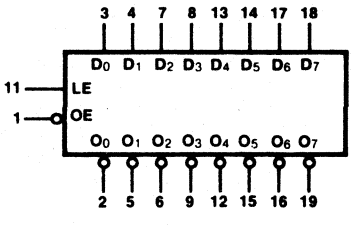
Octal Transparent Latch 54F/74F533

(With 3-State Outputs)

Description — The 'F533 contains eight D-type latches with inverted 3-state outputs for bus organized applications. When the common Latch Enable input is HIGH the latches are transparent, i.e. an output will change state each time its D input changes. When LE is LOW, the data that meets the recommended setup and hold times is latched. A HIGH signal on the common Output Enable input forces the outputs to the high impedance state but does not affect the state of the latches or subsequent data entry. The 'F533 is the same as the 'F373 except that the outputs are inverted.

Inverted 3-State Outputs
D-Type Inputs
Transparent Latches
Propagation Delay 8.0 ns Typ
Supply Current 46 mA Typ

Logic Symbol



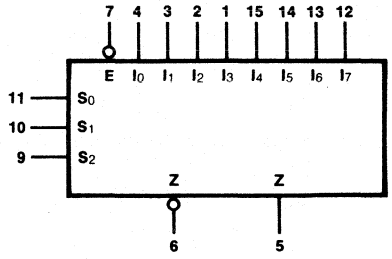
V_{CC} = Pin 20
GND = Pin 10

8-Input Multiplexer 54F/74F151

Description — The 'F151 is a high speed 8-input digital multiplexer with complementary outputs. It can select one line of data from up to eight sources. Signals on the Select inputs S_0 — S_2 determine which of the inputs is routed to the output. A LOW signal on the Enable input $\overline{E}$ allows the Z output to follow the selected input. A HIGH on $\overline{E}$ forces the Z output LOW and $\overline{Z}$ HIGH.

Complementary Outputs
Propagation Delay 6.3 and 8.1 ns Typ
Supply Current 11 mA Typ

Logic Symbol



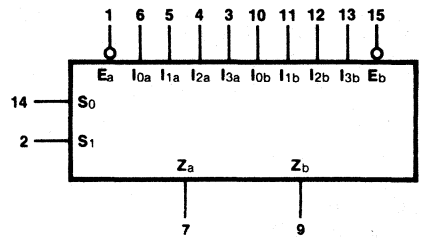
V_{CC} = Pin 16
GND = Pin 8

Dual 4-Input Multiplexer 54F/74F153

Description — The 'F153 contains two 4-input multiplexers with common Select inputs and separate Enable inputs. Signals applied to the Select inputs determine, within each section, which of the four data inputs is routed to the output. A LOW signal on an Enable input allows the output to follow the selected input. A HIGH signal on an Enable forces the output LOW.

Separate Enable Inputs
Common Select Inputs
Propagation Delay 7.9 ns Typ
Supply Current 12 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

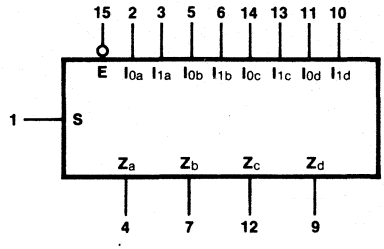
Quad 2-Input Multiplexer

54F/74F157

Description — The 'F157 contains four 2-input multiplexers with common Select and Enable inputs. It can select four bits of data from either of two sources. A LOW signal on the Enable input allows the selected data to be routed to the output. A HIGH signal on the Enable forces the outputs LOW.

Common Select Input
Common Enable Input
Propagation Delay 7.9 ns Typ
Supply Current 15 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

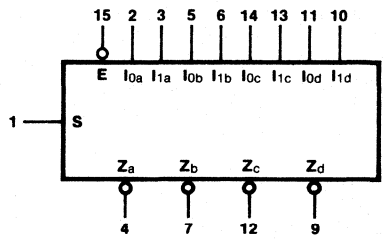
Quad 2-Input Multiplexer

54F/74F158

Description — The 'F158 contains four 2-input multiplexers with common Select and Enable inputs and with inverting outputs. It selects four bits of data from either of two sources. A LOW signal on the Enable input allows the selected data to be routed to the outputs. A HIGH signal on the Enable forces the outputs HIGH.

Inverting Outputs
Common Select Input
Common Enable Input
Propagation Delay 6.3 ns Typ
Supply Current 10 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

8-Input Multiplexer

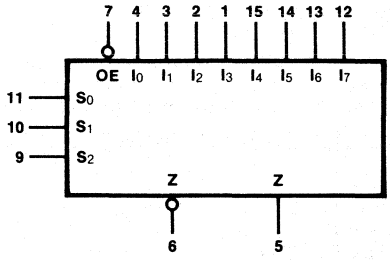
(With 3-State Outputs)

54F/74F251

Description — The 'F251 is a high speed 8-input multiplexer with complementary 3-state outputs. It provides the capability of selecting one line of data from up to eight sources, as determined by signals applied to the Select inputs $\overline{S_0}$ — $\overline{S_2}$. A LOW signal on the Output Enable input $\overline{OE}$ allows the Z output to follow the selected input. A HIGH signal on $\overline{OE}$ forces both outputs to the high impedance state.

Complementary 3-State Outputs
Propagation Delay 2.9 or 4.7 ns Typ
Supply Current 10.5 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Dual 4-Input Multiplexer

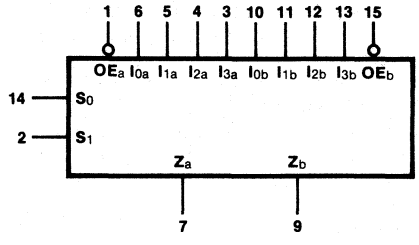
(With 3-State Outputs)

54F/74F253

Description — The 'F253 contains two 4-input multiplexers with common Select inputs, separate Output Enable ($\overline{OE}$) and 3-state outputs. Signals applied to the Select inputs determine, in each section, which of the four data inputs is routed to the output. A LOW signal on $\overline{OE}$ allows the output to follow the selected input. A HIGH on $\overline{OE}$ forces the output to the high impedance state. Outputs are thus capable of interfacing directly with bus oriented systems.

3-State Outputs
Common Select Inputs
Separate Enable Inputs
Propagation Delay 4.5 ns Typ
Supply Current 12.5 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Quad 2-Input Multiplexer

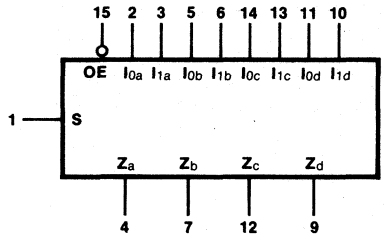
(With 3-State Outputs)

54F/74F257

Description — The 'F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input; therefore, the outputs can interface directly with bus oriented systems.

3-State Outputs
Common Select Input
Common Enable Input
Propagation Delay 4.5 ns Typ
Supply Current 14.6 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Quad 2-Input Multiplexer

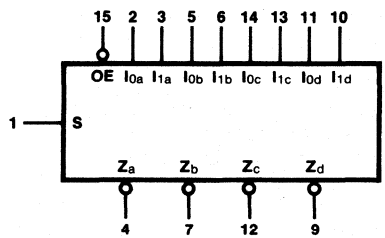
(With 3-State Outputs)

54F/74F258

Description — The 'F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input; therefore, the outputs can interface directly with bus oriented systems. The 'F258 is the same as the 'F257 except that the outputs are inverted.

Inverting 3-State Outputs
Common Select Input
Common Enable Input
Propagation Delay 2.9 ns Typ
Supply Current 14 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

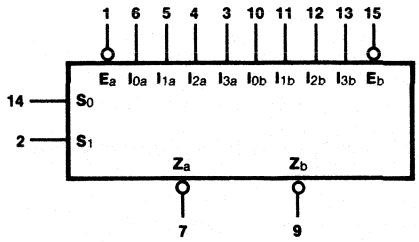
Dual 4-Input Multiplexer

54F/74F352

Description — The 'F352 contains two inverting 4-input multiplexers with common Select inputs and separate Enable inputs. Signals applied to the Select inputs determine, within each section, which of the four data inputs is routed to the output. A HIGH signal on an Enable input forces the related output HIGH. The 'F352 is the functional equivalent of the 'F153 with inverted outputs.

Inverting Outputs
Common Select Inputs
Separate Enable Inputs
Propagation Delay 6.3 ns Typ
Supply Current 8.0 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Dual 4-Input Multiplexer

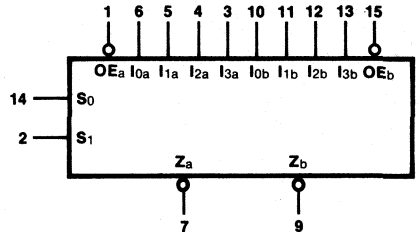
(With 3-State Outputs)

54F/74F353

Description — The 'F353 is a dual 4-input multiplexer with inverting 3-state outputs. It selects two bits of data from any four of sources using common Select inputs. An output can be switched to the high impedance state by a HIGH signal on the respective Output Enable input. Outputs are thus capable of interfacing directly with bus oriented systems. The 'F353 is the functional equivalent of the 'F253 with inverted outputs.

Inverting 3-State Outputs
Common Select Inputs
Separate Enable inputs
Propagation Delay 6.3 ns Typ
Supply Current 13.5 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

1-of-10 Decoder

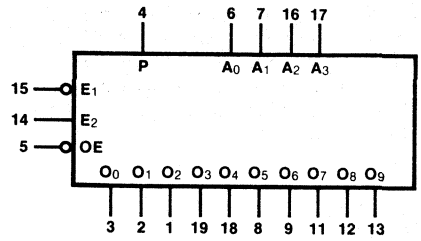
(With 3-State Outputs)

54F/74F537

Description — The 'F537 is a one-of-ten decoder/demultiplexer with four active-HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active-LOW or active-HIGH. The 'F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input enables, active-HIGH E_2 and active-LOW $\overline{E}_1$, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

Output Polarity Control
Complementary Input Enables
3-State Outputs
Ignores Input Codes Above Nine
Address Delay 12 ns Typ
Enable Delay 11 ns Typ
Supply Current 44 ns Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

1-of-8 Decoder

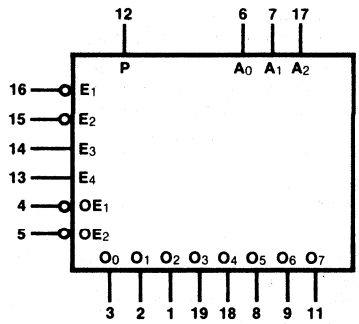
(With 3-State Outputs)

54F/74F538

Description — The 'F538 decoder/demultiplexer accepts three Address (A_0 — A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active-LOW or active-HIGH. A HIGH signal on either of the active-LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active-HIGH and two active-LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to one of eight or one of 16 destinations.

Output Polarity Control
Data Demultiplexing Capability
Multiple Enables for Expansion
3-State Outputs
Address Delay 12 ns Typ
Enable Delay 11 ns Typ
Supply Current 38 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

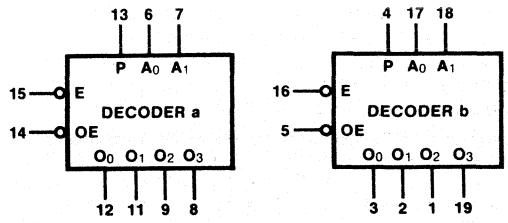
Dual 1-of-4 Decoder 54F/74F539

(With 3-State Outputs)

Description — The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active-HIGH (P = L) or active-LOW (P = H). An active-LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active-LOW mode or in inverted form in the active-HIGH mode. A HIGH signal on the active-LOW Output Enable ($\overline{OE}$) input forces the 3-state outputs to the high impedance state.

Two Functionally Independent Decoders
Output Polarity Control
Input Enable for Demultiplexing
3-State Outputs
Address Delay 12 ns Typ
Enable Delay 11 ns Typ
Supply Current 42 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

4-Bit Bidirectional Universal Shift Register

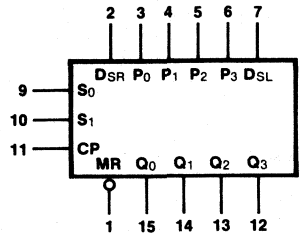
54F/74F194

Description — The 'F194 is a high speed 4-bit bidirectional shift register. Signals applied to the Select (S_0, S_1) inputs determine the mode of operation — shift left, shift right, parallel entry or hold. Except for the reset function, the 'F194 is fully synchronous and state changes are initiated by the rising edge of the clock. The flip-flops are edge-triggered and the inputs can change when the clock is in either state, provided that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on the Master Reset ($\overline{MR}$) input overrides clocked operations and forces the outputs LOW. The circuit is useful for serial-in, serial/parallel-out or parallel-in, serial/parallel-out applications.

Serial and Parallel Entry Ports
Synchronous Serial and Parallel Operation
Fully Edge-Triggered
Asynchronous Master Reset
Shift Frequency 100 MHz Typ

Propagation Delay 7.0 ns Typ
Supply Current 26 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

8-Input Universal Shift/Storage Register

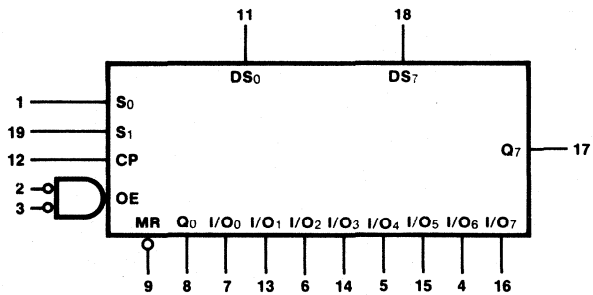
(With Common Parallel I/O Pins)

54F/74F299

Description — The 'F299 is an 8-bit register with multiplexed 3-state I/O ports for bus oriented parallel operations and with separate serial inputs and outputs for expansion. Signals applied to the Select (S_0, S_1) inputs determine the mode of operation — shift left, shift right, parallel entry or hold. State changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed, relative to the clock rising edge. An active-LOW Master Reset input overrides clocked operations and clears the register. A HIGH signal on either Output Enable ($\overline{OE}$) input forces the I/O pins to the high impedance state but does not interfere with other operations.

Multiplexed Parallel I/O Ports
Separate Serial Inputs and Outputs
Expandable Bidirectional Shifting
3-State Outputs for Bus Applications
Shift Frequency 80 MHz Typ
Propagation Delay 9.0 ns Typ
Supply Current 68 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

8-Bit Serial/Parallel Register

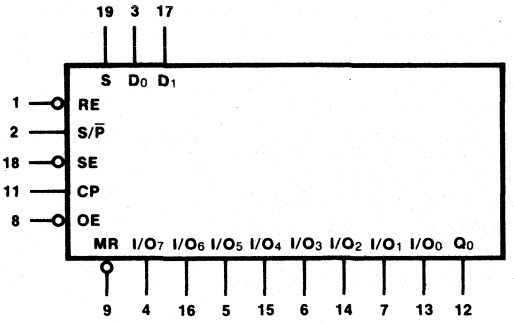
(With Sign Extend)

54F/74F322

Description — The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with signal extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the I/O pins to the high impedance state but does not interfere with other operations. The 'F322 operates with the 'LS384 Multiplier and provides the sign extend function for twos complement arithmetic.

Multiplexed Parallel I/O Ports
Separate Serial Input and Output
Sign Extend Function
3-State Outputs for Bus Applications
Shift Frequency 80 MHz Typ
Propagation Delay 9.0 ns Typ
Supply Current 70 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

8-Bit Universal Shift/Storage Register

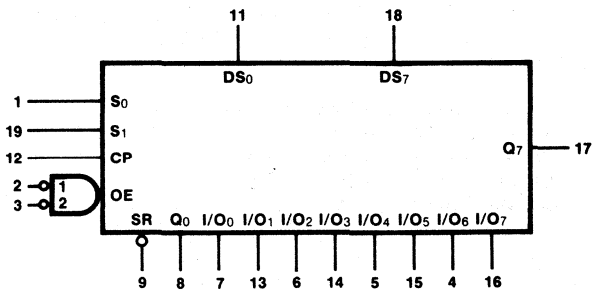
(With Synchronous Reset and Common I/O Pins)

54F/74F323

Description — The 'F323 is an 8-bit universal shift/register with 3-state outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load. The flip-flops are edge-triggered and state changes are initiated by the rising edge of the clock.

Multiplexed Parallel I/O Ports
Separate Serial Inputs and Outputs
Expandable Bidirectional Shifting
3-State Outputs for Bus Applications
Shift Frequency 80 MHz Typ
Propagation Delay 9.0 ns Typ
Supply Current 66 mA Typ

Logic Symbol



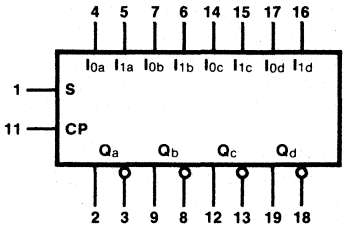
V_{CC} = Pin 20
GND = Pin 10

Quad 2-Port Register **54F/74F398**

Description — The 'F398 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. Both the true and complement outputs of the flip-flops are available.

Select Inputs from Two Sources
Fully Edge-Triggered
True and Complement Outputs
Propagation Delay 6.3 ns Typ
Clock Frequency 150 MHz Typ
Supply Current 21 mA Typ

Logic Symbol



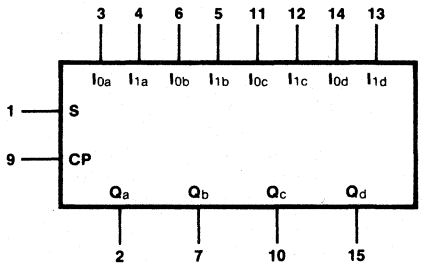
V_{CC} = Pin 20
GND = Pin 10

Quad 2-Port Register **54F/74F399**

Description — The 'F399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

Select Inputs from Two Sources
Fully Edge-Triggered
Propagation Delay 6.3 ns Typ
Clock Frequency 150 MHz Typ
Supply Current 21 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

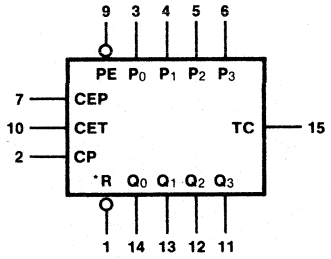
Synchronous Presettable BCD Decade Counter

54F/74F160
54F/74F162

Description — The 'F160 and 'F162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

Synchronous Counting and Loading
High Speed Synchronous Expansion
Propagation Delay 7.5 ns Typ
Count Frequency 120 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8
*MR for '160
*SR for '162

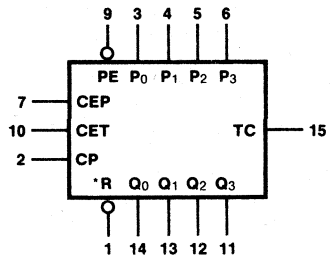
Synchronous Presettable Binary Counter

54F/74F161
54F/74F163

Description — The 'F161 and 'F163 are high speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Synchronous Counting and Loading
High Speed Synchronous Expansion
Propagation Delay 7.5 ns Typ
Count Frequency 120 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8
*MR for '161
*SR for '163

Up/Down Decade Counter

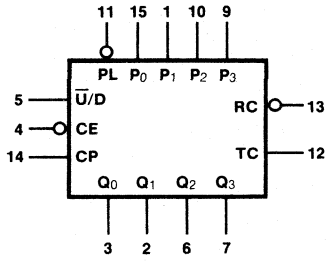
54F/74F190

(With Preset and Ripple Clock)

Description — The 'F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock. The Count Enable and Up/Down control inputs can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Synchronous Counting
Asynchronous Parallel Load
Propagation Delay 10 ns Typ
Count Frequency 70 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Binary Counter

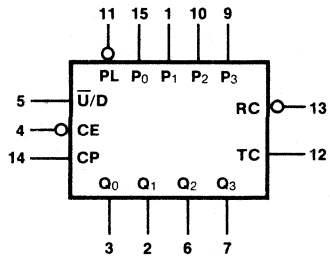
54F/74F191

(With Preset and Ripple Clock)

Description — The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are intiated by the rising edge of the clock. The Count Enable and Up/Down control inputs can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Synchronous Counting
Asynchronous Parallel Load
Propagation Delay 10 ns Typ
Count Frequency 70 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Decade Counter

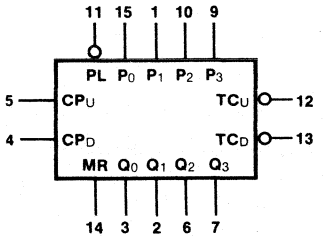
54F/74F192

(With Separate Up/Down Clocks)

Description — The 'F192 is a reversible BCD decade (8421) counter featuring synchronous counting and asynchronous parallel loading. Separate Count Up and Count Down clock inputs determine the direction of counting and in either mode the circuits operate synchronously. State changes are initiated by the rising edge of the clock. Separate Terminal Count Up (carry) and Terminal Count Down (borrow) outputs are gated clocks for a subsequent stage, thus simplifying multistage counter designs. Preset data inputs make the 'F192 useful in programmable counters. The Parallel Load ($\overline{PL}$) input overrides counting, while the Master Reset (MR) input overrides both counting and parallel loading.

Separate Up and Down Clocks
Asynchronous Parallel Loading
Carry and Borrow Outputs for Cascading
Propagation Delay 6.5 ns Typ
Count Frequency 70 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Binary Counter

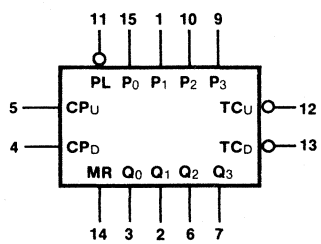
54F/74F193

(With Separate Up/Down Clocks)

Description — The 'F193 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous parallel loading. Separate Count Up and Count Down clocks determine the direction of counting and in either mode the circuits operate synchronously. State changes are initiated by the rising edge of the clock. Separate Teminal Count Up (carry) and Terminal Count Down (borrow) outputs are gated clocks that need no external logic to serve as clocks for a subsequent stage, thus simplifying multistage counter designs. Preset data inputs make the 'F193 useful in programmable counters. The Parallel Load ($\overline{PL}$) input overrides counting, while the Master Reset (MR) input overrides both counting and parallel loading.

Separate Up and Down Clocks
Asynchronous Parallel Loading
Carry and Borrow Outputs for Cascading
Propagation Delay 6.5 ns Typ
Count Frequency 70 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

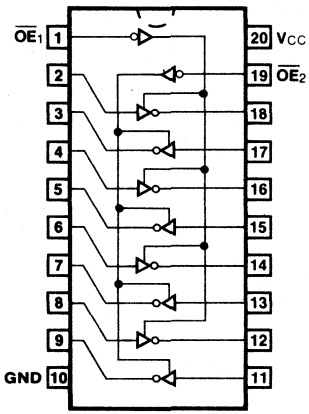
Octal Buffer/Line Driver 54F/74F240

(With 3-State Outputs)

Description — The 'F240 contains eight inverting buffers with 3-state outputs. They offer improved PC board density and are well suited as memory address drivers, clock drivers and bus oriented transmitters or receivers. The 'F240 has a pair of active-LOW Output Enable ($\overline{OE}$) inputs, each of which controls four of the buffers. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Inverting Buffers
Separate 4-Bit Enables
Output Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 4.5 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

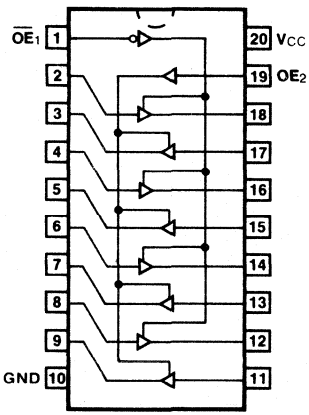
Octal Buffer/Line Driver 54F/74F241

(With 3-State Outputs)

Description — The 'F241 contains eight non-inverting buffers with 3-state outputs. Four of the buffers are controlled by an active-HIGH Output Enable (OE) input and four are controlled by an active-LOW $\overline{OE}$ input. This makes them well suited for pairing in transceiver applications. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Non-Inverting Buffers
Opposite Polarity 4-Bit Enables
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 6.0 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

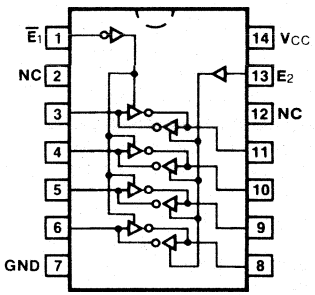
Quad Bus Transceiver 54F/74F242

(With 3-State Outputs)

Description — The 'F242 contains four inverting transceivers with 3-state outputs. They are designed for 4-line asynchronous 2-way communication between data or control busses. An active-LOW Output Enable ($\overline{OE}$) input controls data flow in one direction; an active-HIGH OE input controls data flow in the other direction. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Inverting Buffers
2-Way Bus Communication
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 4.5 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

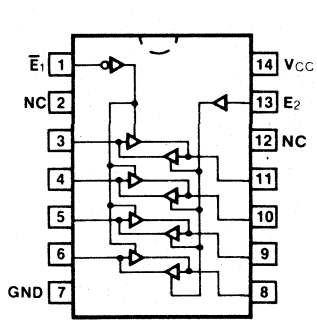
Quad Bus Transceiver 54F/74F243

(With 3-State Outputs)

Description — The 'F243 contains four non-inverting transceivers with 3-state outputs. They are designed for 4-line asynchronous 2-way communication between data or control busses. An active-LOW Output Enable ($\overline{OE}$) input controls data flow in one direction; an active-HIGH OE input controls data flow in the other direction. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Non-Inverting Buffers
2-Way Bus Communication
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 6.0 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

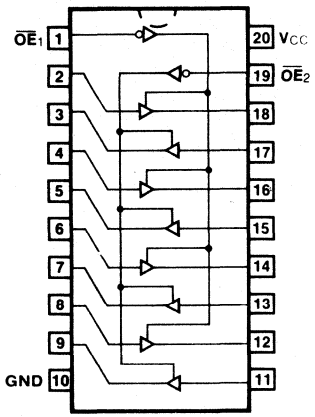
Octal Buffer/Line Driver 54F/74F244

(With 3-State Outputs)

Description — The 'F244 contains eight non-inverting buffers with 3-state outputs. They offer improved PC board density and are well suited as memory address drivers, clock drivers and bus oriented transmitters or receivers. The 'F244 has a pair of active-LOW Output Enable ($\overline{OE}$) inputs, each of which controls four of the buffers. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Non-Inverting Buffers
Separate 4-Bit Enables
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 6.0 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

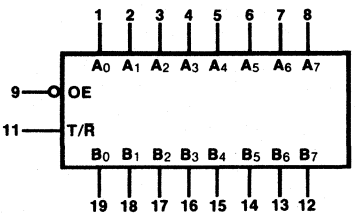
Octal Bidirectional Transceiver 54F/74F545

(With 3-State Inputs/Outputs)

Description — The 'F545 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a 3-state condition. Output HIGH voltage V_{OH} is specified as 3.6 V for MOS interfacing.

Non-Inverting Buffers
Bidirectional Data Path
B Outputs Sink 64 mA, Source 15 mA
V_{OH} Specified as 3.6 V at 0.4 mA
Propagation Delay 6.0 ns Typ
Supply Current 128 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

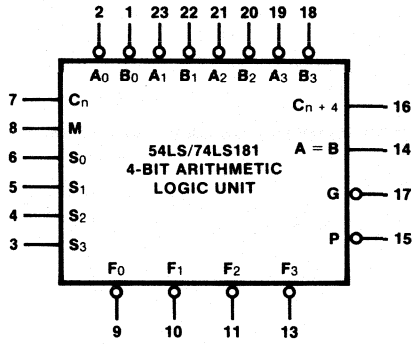
4-Bit Arithmetic Logic Unit

54F/74F181

Description — The 'F181 is a 4-bit Arithmetic Logic Unit capable of performing 16 arithmetic or 16 logic operations on two 4-bit operands $A_0 — A_3$ and $B_0 — B_3$. The Carry Out (C_{n+4}) output is provided for ripple carry expansion, while the Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs can be used with an 'F182 or similar Carry Lookahead Generators for faster operations on longer words. The Mode Control (M) input determines whether a logic (M = H) or an arithmetic (M = L) operation is performed. Signals applied to the Select ($S_0 — S_3$) inputs determine the specific function or operation.

Performs 16 Arithmetic Operations
Performs 16 Logic Functions
Internal Lookahead for Fast Ripple Carry
$\overline{G}$ and $\overline{P}$ Outputs for External Lookahead
A or B to Carry Delay 10 ns Typ
Ex-OR Logic Delay 8.7 ns Typ
Supply Current 39 mA Typ

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

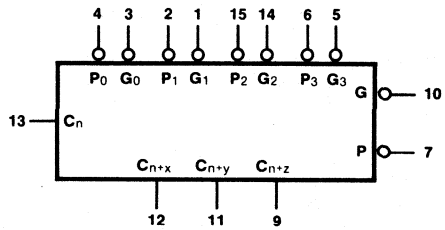
Carry Lookahead Generator

54F/74F182

Description — The 'F182 is a high-speed carry lookahead generator for use with the 'F181, 'F381, 2901A or other 4-bit ALUs in arithmetic operations on words longer than four bits. It accepts up to four pairs of active-LOW Carry Propagate ($\overline{P}_0 — \overline{P}_3$) and Carry Generate ($\overline{G}_0 — \overline{G}_3$) signals, an active-HIGH *Carry input* (C_n) *and provides anticipated active-*HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four ALUs. It also has active-LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs for optional use in further levels of lookahead. The 'F182 works equally well when the ALU operand inputs follow either the active-LOW or the active-HIGH convention.

Provides Lookahead Across Four ALUs
Multi-Level Capability for Longer Words
Less Loading of ALU Outputs
Propagation Delay 4.6 ns Typ
Supply Current 19 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

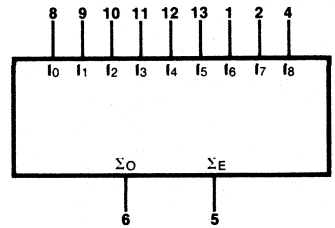
9-Bit Parity Generator/Checker

54F/74F280

Description — The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether the number of HIGH inputs is even or odd. If even, the Sum Even output is HIGH; if odd, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output. For longer words, the Sum Even output is used as an input to the next package.

Nine Input Lines
Odd or Even Parity
Propagation Delay 12.5 ns Typ
Supply Current 25 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

4-Bit Binary Full Adder

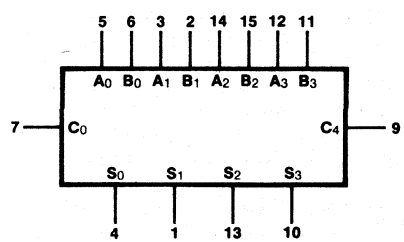
(With Fast Carry)

54F/74F283

Description — The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words ($A_0 — A_3$, $B_0 — B_3$) and a Carry input (C_0). It generates the binary Sum outputs ($S_0 — S_3$) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

Adds Two 4-Bit Numbers
Full Internal Carry Lookahead
Fast Ripple Carry for Economical Expansion
Ripple Carry Delay 4.7 ns Typ
Sum Output Delay 8.5 Typ
Supply Current 30 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

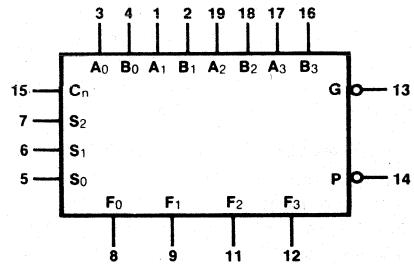
4-Bit Arithmetic Logic Unit

54F/74F381

Description — The 'F381 is a 20-pin ALU that performs three arithmetic operations (A plus B, A minus B, B minus A) and three logic functions (AND, OR, Exclusive-OR) on two 4-bit words, A and B. Two additional Select input codes force the *Function* ($F_0 - F_3$) *outputs LOW or HIGH. Carry* Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, please refer to the 'F382 ALU.

20-Pin Space-Saving Package
Minimum Input Drive Required
Performs Eight Functions
$\overline{P}$ and $\overline{G}$ Outputs for Expansion
Subtract Delay 8.5 ns Typ
Lookahead Delay 7.6 ns Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

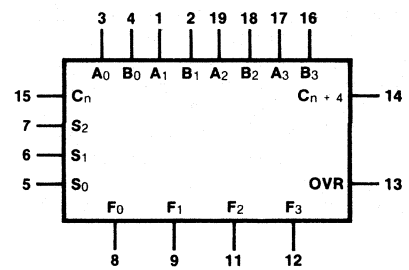
4-Bit Arithmetic Logic Unit

54F/74F382

Description — The 'F382 is a 20-pin ALU that performs three arithmetic operations (A plus B, A minus B, B minus A) and three logic functions (AND, OR, Exclusive-OR) on two 4-bit words, A and B. Two additional Select input codes force the Function ($F_0 - F_3$) outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, please refer to the 'F381.

20-Pin Space-Saving Package
Minimum Input Drive Required
Performs Eight Functions
Ripple Carry and Overflow Outputs
A or B to Carry Output Delay 10 ns Typ
Select to Output Delay 14.5 ns Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

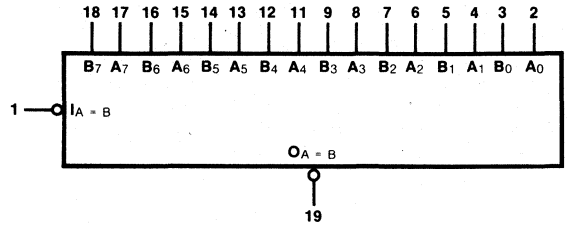
8-Bit Identity Comparator

54F/74F521

Description — The 'F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. For longer words, two or more packages can be cascaded by means of the $\overline{I}_{A=B}$ input , which also serves as an active-LOW enable input.

Compares Two 8-Bit Words
Expandable for Longer Words
Space-Saving 20-Pin Package
Propagation Delay 7.5 ns Typ
Supply Current 28 mA Typ

Logic Symbol



VCC = Pin 20
GND = Pin 10

8-Bit by 8-Bit Multiplier

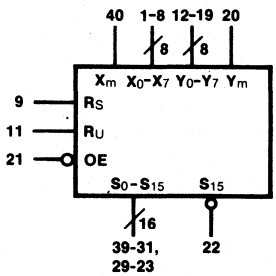
54F/74F558

(With 3-State Outputs)

Description — The 'F558 is a high-speed combinatorial array that multiplies two 8-bit unsigned or signed twos complement numbers and provides the 16-bit unsiged or signed product. Each input operand X and Y has a mode control input that determines whether the number is treated as signed or unsigned. Two additional inputs, R_S and R_U, allow the addition of a bit for rounding to the best signed or unsiged fractional 8-bit result. For expansion during signed or mixed multiplication, both the true and complement outputs of the most significant bit are available.

Unsigned, Signed or Mixed Multiplication
Full 16-Bit Product Outputs
MSB Complement Output for Signed Expansion
Rounding Inputs for Fractional 8-Bit Product
Propagation Delay 50 ns Typ
Supply Current 200 mA Typ

Logic Symbol



VCC = Pin 10
GND = Pin 30

Expandable 8-Bit Twos Complement Multiplier/Divider

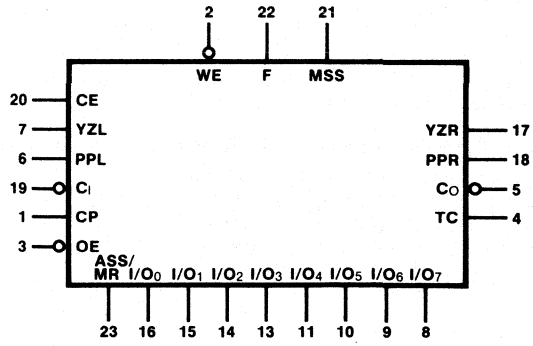
(With 3-State Outputs)

54F/74F559

Description — The 'F559 implements fast signed twos complement multiplication and division as an asynchronous peripheral in microprocessor and minicomputer systems. It contains an 8-bit ALU, three 8-bit registers, a 4-bit sequence counter and the control logic necessary to perform multiply, rounded multiply, fractional divide and integer divide operations. The two 8-bit operands are entered successively at the I/O ports, whereupon the circuit operates internally at a rate determined by an externally applied clock frequency of up to 25 MHz. Upon completion, and upon command, results are presented at the I/O ports in successive 8-bit words. Linking inputs and outputs are provided for expansion to longer words by using two or more multipliers operating on the same 8-bit bus.

Signed Twos Complement Arithmetic
Increases Processor Efficiency
Low System Parts Count
Expandable in 8-Bit Increments
8-Bit Bus Oriented 3-State I/O
16-Bit Multiply in 1.2 μs Typ
16-Bit Divide in 1.6 μs Typ

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

64-Bit Random Access Memory

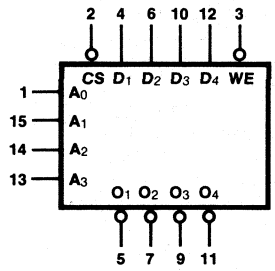
(With 3-State Outputs)

54F/74F189

Description — The 'F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

3-State Outputs for Bus Applications
Buffered Inputs for Minimum Loading
Address Decoding On-Chip
Address Access Time 20 ns Typ
Chip Select Access Time 12 ns Typ
Supply Current 43 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

64-Bit Random Access Memory

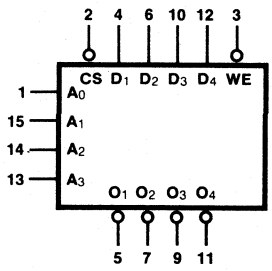
(With Open-Collector Outputs)

54F/74F289

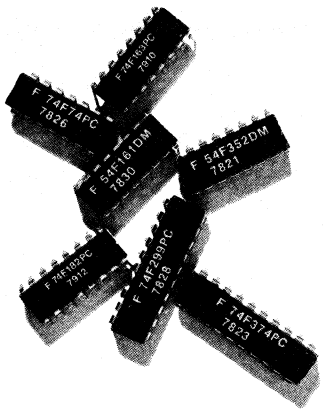
Description — The 'F289 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

Open-Collector Outputs
Buffered Inputs Minimize Loading
Address Decoding On-Chip
Address Access Time 20 ns Typ
Chip Select Access Time 12 ns Typ
Supply Current 43 mA Typ

Logic Symbol



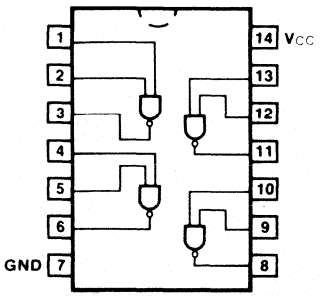
V_{CC} = Pin 16
GND = Pin 8



54F/74F00

QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F00PC		9A
Ceramic DIP (D)	74F00DC	54F00DM	6A
Flatpak (F)	74F00FC	54F00FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			2.8 10.2	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

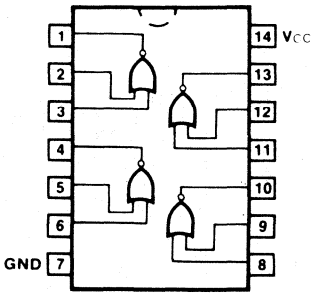
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	2.9 2.6	3.9 3.6	2.0 2.0	7.0 6.5	2.0 2.0	6.0 5.5	ns	2-17 2-18

54F/74F02

QUAD 2-INPUT NOR GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F02PC		9A
Ceramic DIP (D)	74F02DC	54F02DM	6A
Flatpak (F)	74F02FC	54F02FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			5.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				13		*	

AC CHARACTERISITCS: See Section 2 for waveforms and load configurations

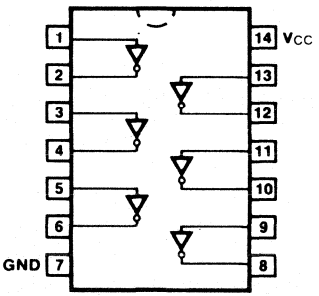
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.0	3.5	4.8	2.5	8.0	2.5	7.0	ns	2-17
t_{PHL}		1.5	2.6	3.5	2.0	6.5	2.0	5.5		2-18

*Measured with one input HIGH, one input LOW for each gate.

54F/74F04

HEX INVERTER

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F04PC		9A
Ceramic DIP (D)	74F04DC	54F04DM	6A
Flatpak (F)	74F04FC	54F04FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC CHARACTERISITCS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			4.2 15.3	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

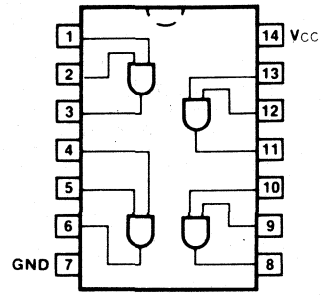
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	2.7 2.5	3.8 3.5	2.0 2.0	7.0 6.5	2.0 2.0	6.0 5.5	ns	2-17 2-18

54F/74F08

QUAD 2-INPUT AND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F08PC		9A
Ceramic DIP (D)	74F08DC	54F08DM	6A
Flatpak (F)	74F08FC	54F08FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISITCS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			8.3	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}				12.9		V_{IN} = Gnd	

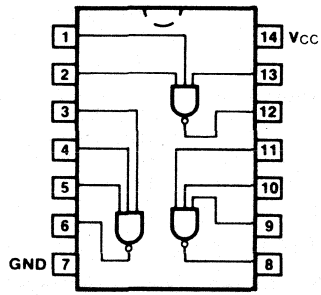
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.0	4.1	5.5	3.0	8.0	3.0	7.0	ns	2-17
t_{PHL}		2.5	3.6	5.0	3.0	7.0	3.0	6.0		2-19

54F/74F10

TRIPLE 3-INPUT NAND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F10PC		9A
Ceramic DIP (D)	74F10DC	54F10DM	6A
Flatpak (F)	74F10FC	54F10FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC CHARACTERISITCS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			2.1 7.7	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max

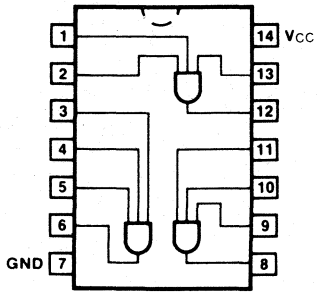
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = 5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	2.9 2.7	3.9 3.7	2.0 2.0	7.0 6.5	2.0 2.0	6.0 5.5	ns	2-17 2-18

54F/74F11

TRIPLE 3-INPUT AND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F11PC		9A
Ceramic DIP (D)	74F11DC	54F11DM	6A
Flatpak (F)	74F11FC	54F11FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			6.2 9.7	mA	V_{IN} = Open V_{IN} = Gnd	V_{CC} = Max

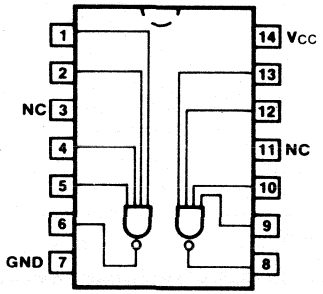
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.5 2.5	4.2 3.7	5.5 5.0	3.0 3.0	8.0 7.0	3.0 3.0	7.0 6.0	ns	2-17 2-19

54F/74F20

DUAL 4-INPUT NAND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F20PC		9A
Ceramic DIP (D)	74F20DC	54F20DM	6A
Flatpak (F)	74F20FC	54F20FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			1.4	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				5.1		V_{IN} = Open	

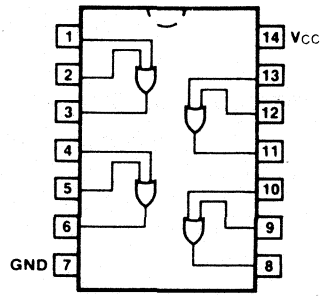
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.5	2.9	3.9	2.0	7.0	2.0	6.0	ns	2-17
t_{PHL}		1.5	2.8	3.8	2.0	6.5	2.0	5.5		2-18

54F/74F32

QUAD 2-INPUT OR GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F32PC		9A
Ceramic DIP (D)	74F32DC	54F32DM	6A
Flatpak (F)	74F32FC	54F32FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			8.3	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}				15.5		V_{IN} = Gnd	

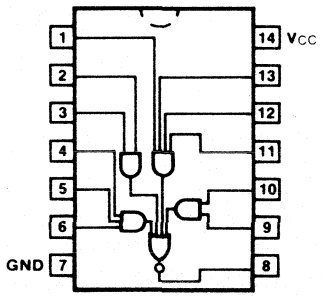
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	3.9	5.5	3.0	8.0	3.0	7.0	ns	2-17
t_{PHL}		2.5	3.5	5.0	3.0	7.0	3.0	6.0		2-19

54F/74F64

4-2-3-2-INPUT AND OR-INVERT GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F64PC		9A
Ceramic DIP (P)	74F64DC	54F64DM	6A
Flatpak (F)	74F64FC	54F64FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			2.8 4.7	mA	V_{IN} = Gnd *	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	3.6 2.8	4.8 3.8	2.0 2.0	8.0 6.5	2.0 2.0	7.0 5.5	ns	2-17 2-18

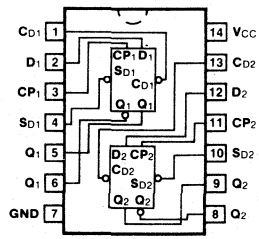
*I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

54F/74F74

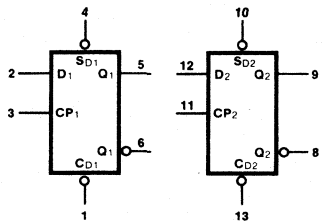
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

CONNECTION DIAGRAM



LOGIC SYMBOL



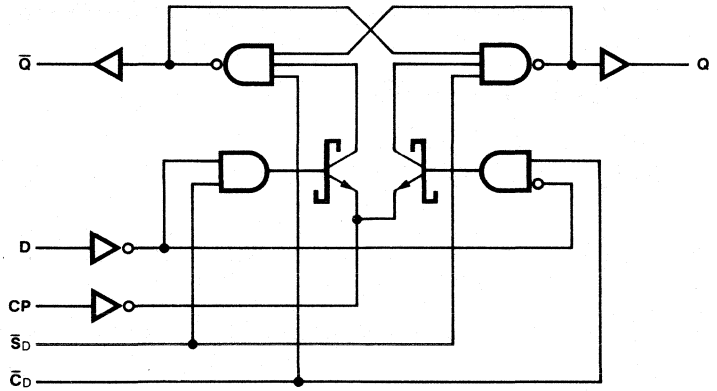
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F74PC		9A
Ceramic DIP (D)	74F74DC	54F74DM	6A
Flatpak (F)	74F74FC	54F74FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F HIGH/LOW
D_1, D_2	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	25/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		10.5		mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency		145						MHz	2-17, 2-21
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$		4.4 4.8						ns	2-17, 2-21
t_{PLH} t_{PHL}	Propagation Delay[1] $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		3.2 4.2						ns	2-17, 2-22
t_{PLH} t_{PHL}	Propagation Delay[2] $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{Q}_n$ or $\overline{Q}_n$		3.4 3.6						ns	2-17, 2-22

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP_n	2.0 3.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP_n	1.0 1.0								
t_w (H) t_w (L)	CP_n Pulse Width, HIGH or LOW	4.0 4.0							ns	2-21
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0							ns	2-22

1. $V_{CP} \geq 2.0$ V 2. $V_{CP} \leq 0.8$ V

54F/74F109

DUAL J$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 'F109 consists of two high speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{K}$ inputs together.

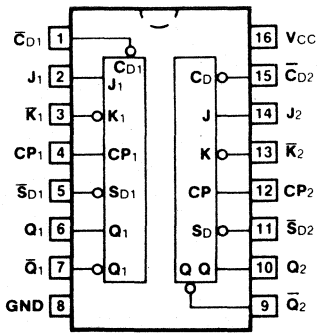
TRUTH TABLE

INPUTS		OUTPUTS
@ t_n		@ t_{n+1}
J	$\overline{K}$	Q $\overline{Q}$
L	H	No Change
L	L	L H
H	H	H L
H	L	Toggles

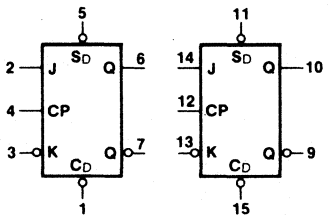
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

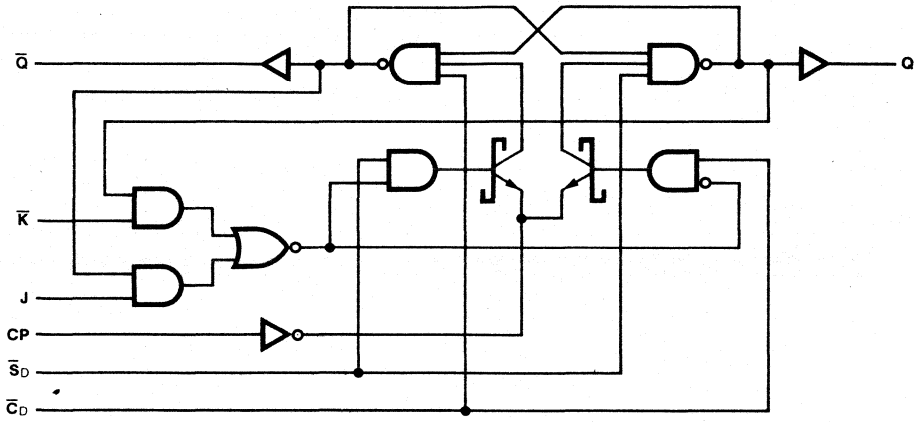
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F109PC		9A
Ceramic DIP (D)	74F109DC	54F109DM	6A
Flatpak (F)	74F109FC	54F109FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		11.7		mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

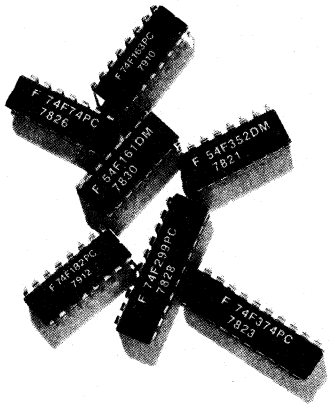
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency		140						MHz	2-17, 2-21
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n to $\overline{Q}_n$		4.4 4.8						ns	2-17, 2-21
t_{PLH} t_{PHL}	Propagation Delay[1] $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		3.2 4.2						ns	2-17, 2-22
t_{PLH} t_{PHL}	Propagation Delay[2] $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		3.4 3.6						ns	2-17, 2-22

1. $V_{CP} \geq 2.0$ V
2. $V_{CP} \leq 0.8$ V

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	2.0 3.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	1.0 1.0								
t_w (H) t_w (L)	CP_n Pulse Width, HIGH or LOW	4.0 4.0							ns	2-21
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0							ns	2-22

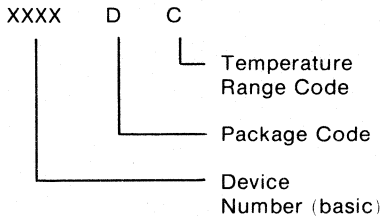
1. $V_{CP} \geq 2.0$ V
2. $V_{CP} \leq 0.8$ V



Section 5

Ordering Information/ Package Outlines

Specific ordering codes, as well as the temperature ranges and package types available, are listed on each data sheet in Section 4. The Product Index/Availability Guide and Selection Guides given in Sections 1 and 3, respectively, list only the "basic device numbers". This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Temperature Range — Two basic temperature grades are in common use:

C = Commercial
0°C to +70°C

M = Military
-55°C to +125°C

Package Code — One letter represents the basic package type. Different package outlines exist within each package type to accommodate varying die sizes and number of pins, as indicated below:

D — Ceramic/Hermetic Dual In-line
4E, 6A, 6B, 6I, 6N, 7B

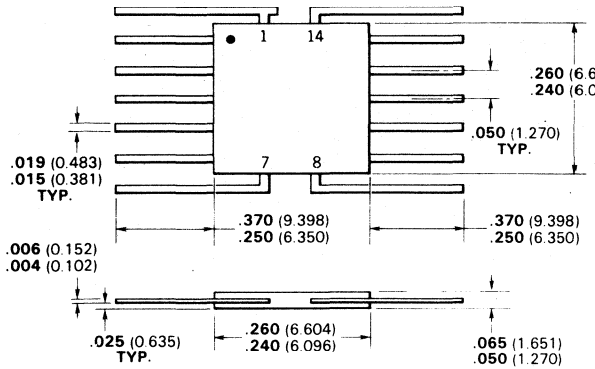
F — Flatpak
3I, 4F, 4L, 4M

P — Plastic Dual In-line
8P, 9A, 9B, 9N, 9Z

Package Outlines — The package outlines indicated by the codes above are shown in the detailed outline drawings in this section.

JEDEC TO-86 Outline

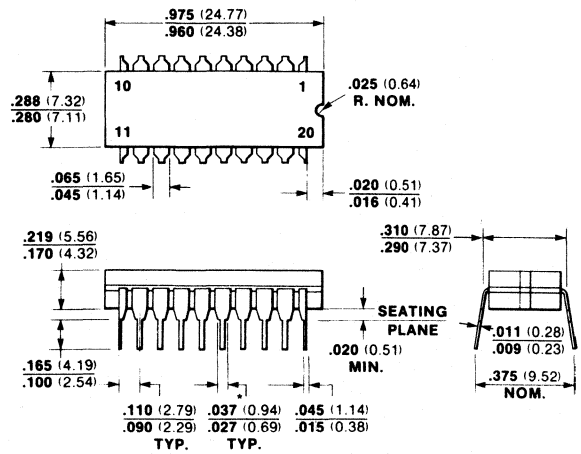
3I



Notes:
Pins are tin-plated 42 alloy
Hermetically sealed alumina package
Pin 1 orientation may be either tab or dot
Cavity size is **.130** (3.30)
Package weight is 0.26 gram

20-Pin CERDIP

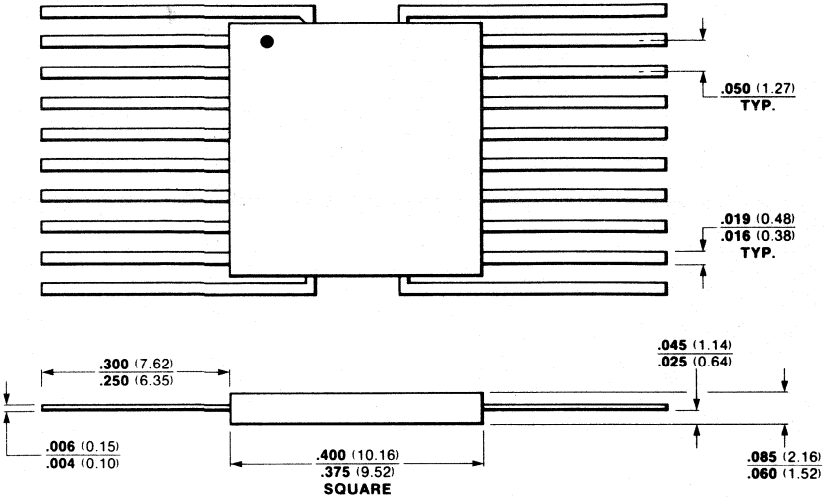
4E



Notes:
Pins are tin-plated kovar or nickel alloy 42
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) diameter pins
Hermetically sealed alumina package (black)
Cavity size is **.140 x .250** (3.56 x 6.35)
*The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.4 grams

All dimensions in inches (bold) and millimeters (parentheses)

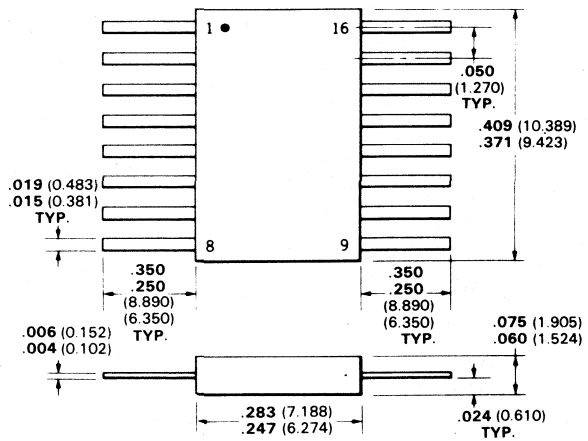
20-Pin CERPAK 4F



Notes:
Pins are tin -plated nickel ally
Base is Al_2O_3
Cavity size **.200 x .200**
Package weight = 0.8 grams

5

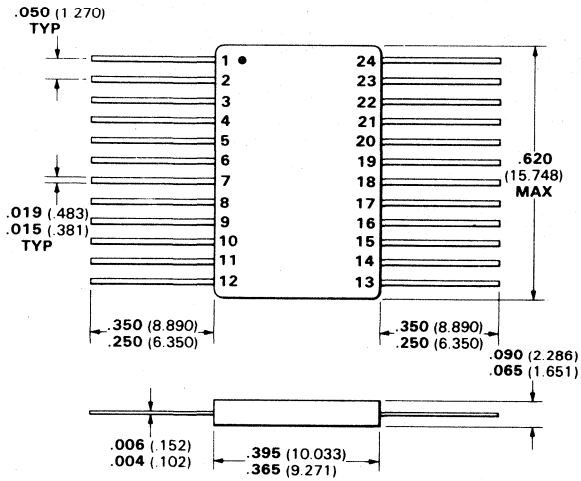
16-Pin BeO CERPAK 4L



Notes:
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

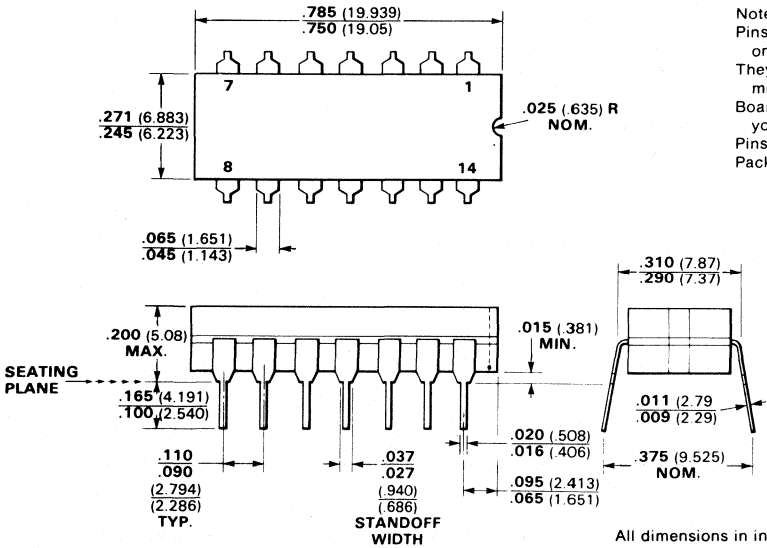
All dimensions in inches (bold) and millimeters (parentheses)

24-Pin CERPAK **4M**



Notes:
Pins are tin-plated nickel alloy
Base is Al_2O_3 or BeO
Cavity size is **.200 x .200**
Package weight is 0.8 grams

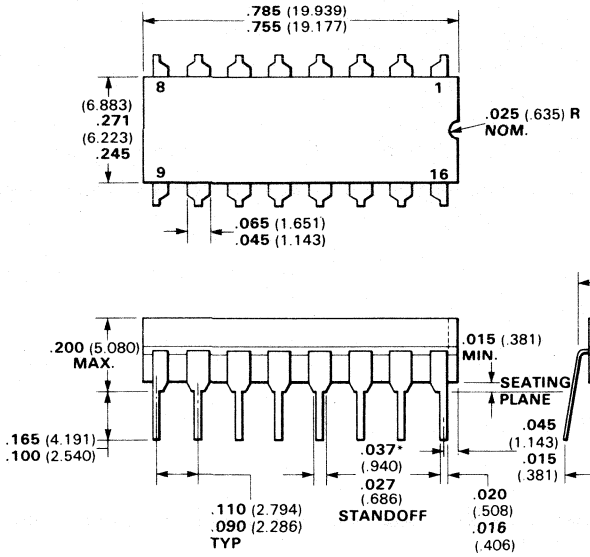
14-Pin Hermetic Dual In-Line (JEDEC TO-116 Outline) **6A**



Notes:
Pins are intended for insertion in hole rows on **.300** (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

All dimensions in inches (bold) and millimeters (parentheses)

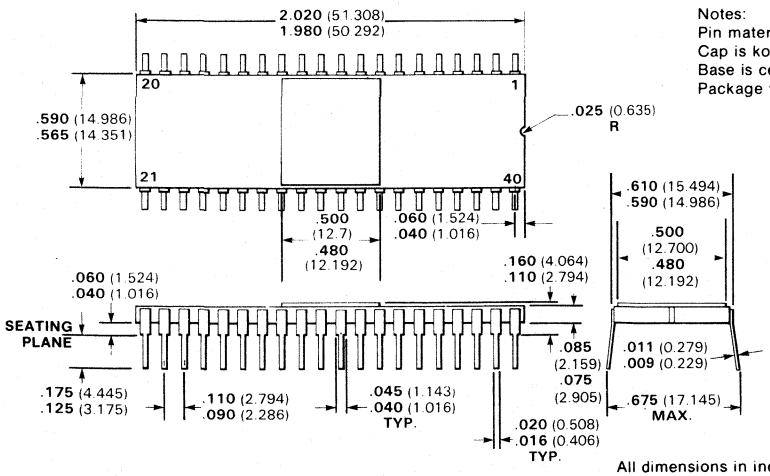
16-Pin Dual In-Line 6B



Notes:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin
Hermetically sealed alumina package
Cavity size is **.110 x .140** (2.79 x 3.56)
Package weight is 2.0 grams
*The **.037-.027** (0.94-069) dimension does not apply to the corner pins

5

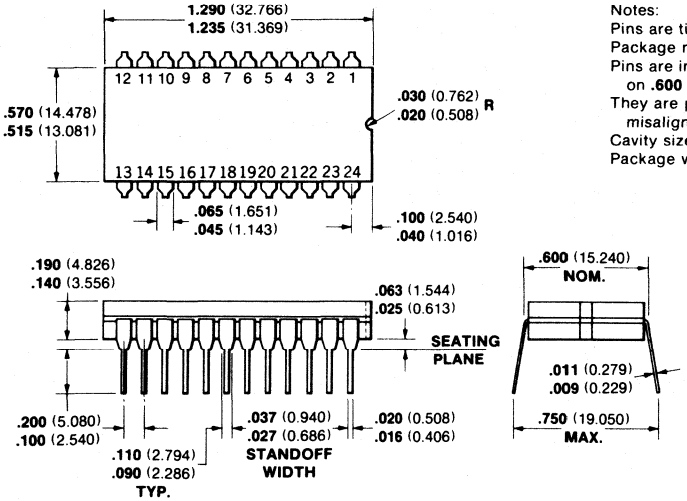
40-Pin Dual In-Line Side-Brazed Dual In-Line 6I



Notes:
Pin material nickel gold-plated kovar
Cap is kovar
Base is ceramic
Package weight is 6.5 grams

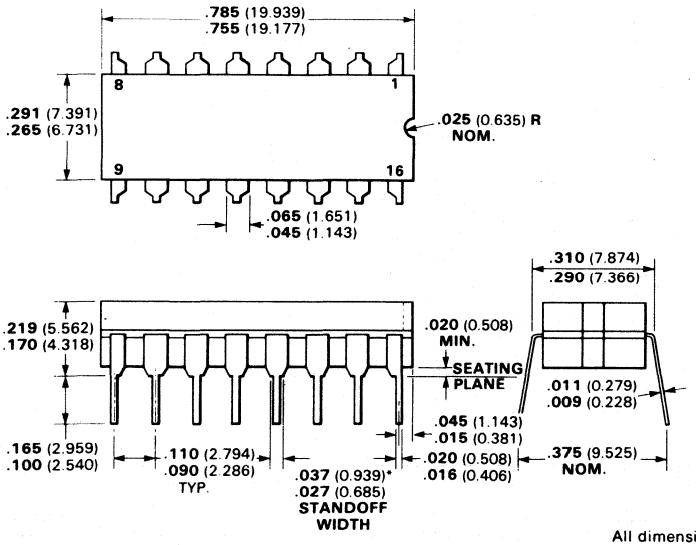
All dimensions in inches (bold) and millimeters (parentheses)

24-Pin Dual In-Line 6N



Notes:
Pins are tin-plated 42 alloy
Package material is alumina
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.230 x .230** (5.84 x 5.84)
Package weight is 6.5 grams

16-Pin Dual In-Line 7B

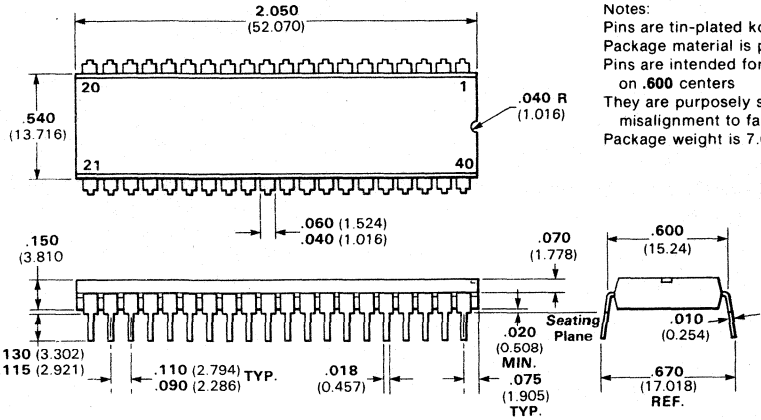


Notes:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin
Hermetically sealed alumina package
Cavity size is **.130 x .230**
*The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams

All dimensions in inches (bold) and millimeters (parentheses)

40-Pin Plastic Dual In-Line

8P

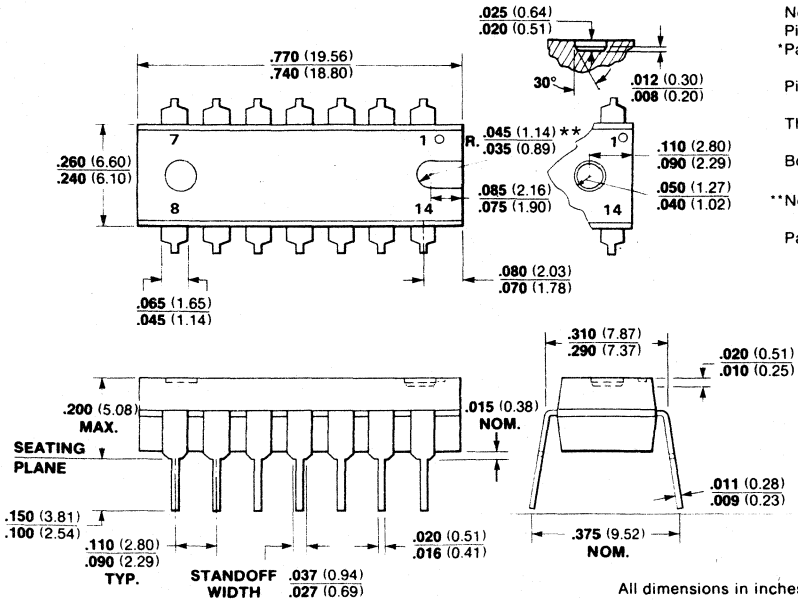


Notes:
Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on **.600** centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 7.0 grams

5

14-Pin Plastic* Dual In-Line (JEDEC TO-116 Outline)

9A

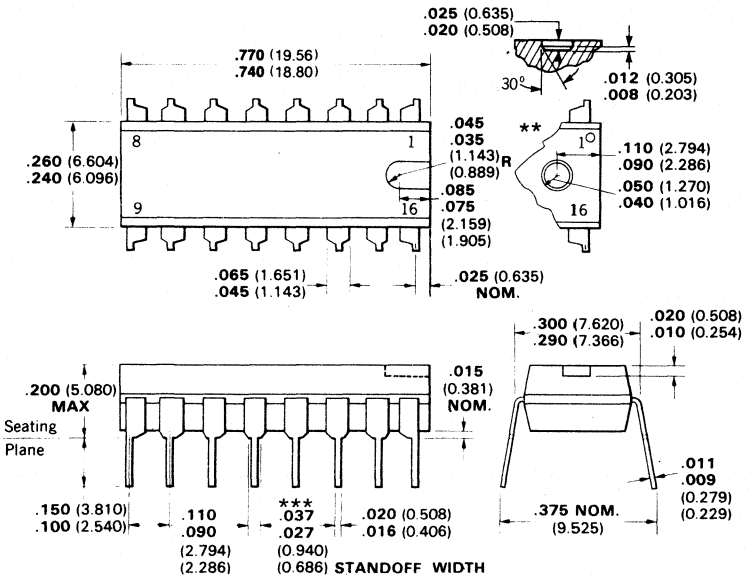


Notes:
Pins are tin-plated kovar
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.508) diameter pin
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 grams

All dimensions in inches (bold) and millimeters (parentheses)

16-Pin Plastic* Dual In-Line

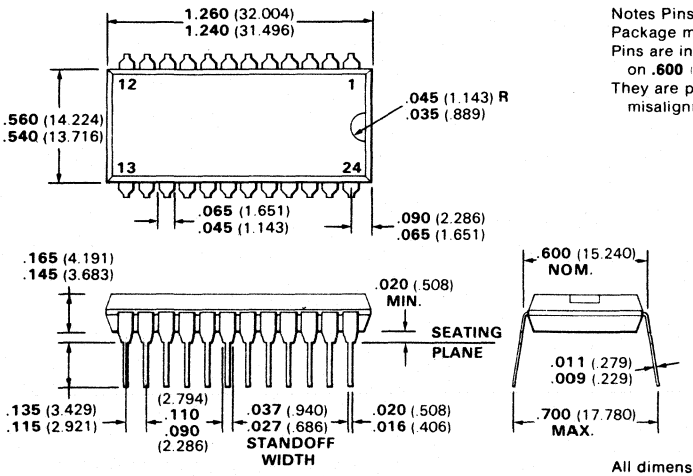
9B



Notes:
Pins are tin-plated kovar or alloy 42 nickel
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.0210** (0.51) diameter pin
Package weight is 0.9 grams
*Package material varies depending on the product line
***The **.037-0.27** (0.94-0.69) dimension does not apply to the corner pins
***Notch or ejector hole varies depending on the product line

24-Pin Plastic Dual In-Line

9N

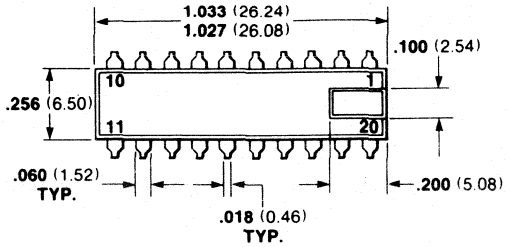


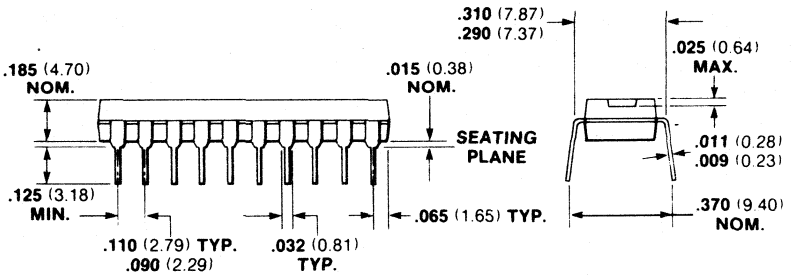
Notes Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion

All dimensions in inches (bold) and millimeters (parentheses)

20-Pin Plastic Dual In-Line

9Z

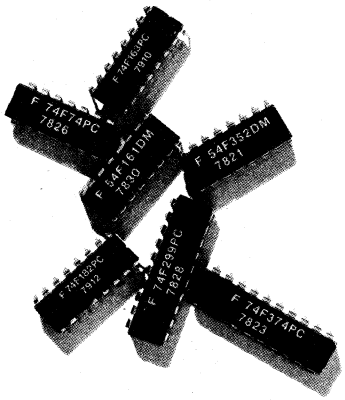




Notes:
Pins are tin-plated alloy 42 copper (olin 195)
Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" *misalignment to facilitate insertion*
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin
Package weight is a little over 1.0 gram

5

All dimensions in inches (bold) and millimeters (parentheses)



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